Introduction to Electronics

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Chapter 1: Introduction

Introduction

The advent of electronics has had a profound impact on our lives and impacted nearly every product that we use either directly or indirectly. Without electronics, present day computers, cell phones, stereos, televisions, and the internet would not be possible. And of course, without computers and modern communications tools, society could not have made the huge strides in fields such as medicine, aerospace technologies, meteorology, transportation, agriculture, education, and many others. It is for these reasons that the invention of the transistor is considered as one of the most important technological advancements in history.

This first chapter provides an overview of what makes electronic circuits different from what you have studied thus far, and some notation that is important to understand as we begin our investigation of electronic devices and circuits.

What are Electronic Circuits

In this booklet, we will examine some simple electronic devices, how to analyze circuits with them, and a few applications that highlight the importance of these devices. When we use the term "electronic circuit" in this booklet, it means that the circuit contains electronic devices such as diodes and/or transistors.

Why Electronics and Why Now?

Why introduce electronics in tandem with circuit analysis? Since most practical circuits contain electronic devices, introducing electronics helps illustrate why studying circuit analysis is important. This study will hopefully make your study of circuit analysis techniques more meaningful because you will get to apply these techniques to real-life circuits.

Electronic Subsystems

Many of the electronic products that you have encountered in your life may seem extremely complex and many of them are. However, engineers break these complex circuits into sub systems or components that can be analyzed separately.

Take for instance a common power supply also known as a power supply or AC to DC converter (see Figure 1). These converters are commonly used with cell phones, laptop computers, cordless phones, televisions, and many other consumer electronic products. The AC to DC converter takes AC voltage from a standard wall outlet and converts it into a DC voltage that powers the product.

Figure 1: Photo of AC to DC Converters

A functional block diagram of such a converter is shown in Figure 2 below. It is relatively easy to understand how each of the components in the system operates and we will investigate these components at the end of Chapter 2.

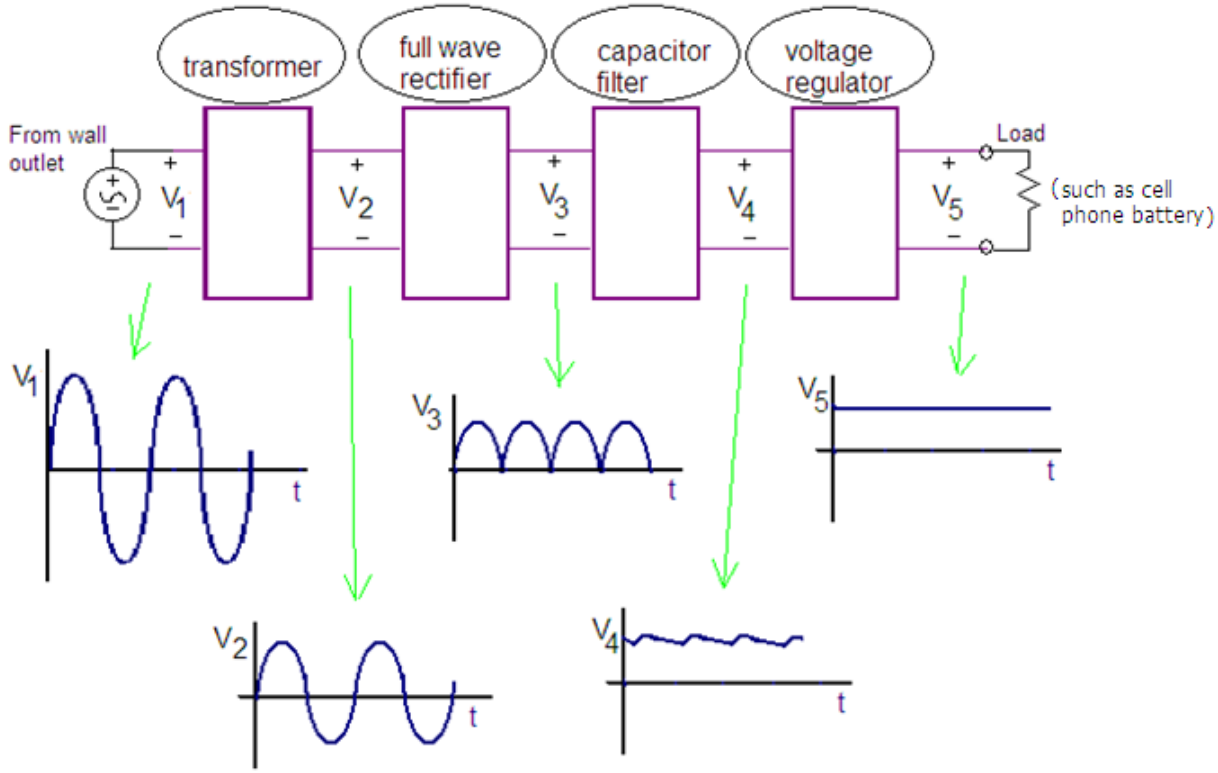


Figure 2: AC to DC Conversion Block Diagram

Another example of a complex electronic system consisting of many subsystems is an FM radio shown as a block diagram in Figure 3. The antenna captures the electromagnetic radio frequency (RF) signal and produces a very weak voltage signal that is sent to the tuner. The tuner takes the incoming RF voltage signal and produces an audio signal by employing a voltage amplifier (to boost the weak signal from the antenna), filter circuitry (to select the desired radio station), and a

demodulator that converts the RF signal into an audio frequency (sound) signal. The PreAmp amplifies (increases the voltage amplitude) of this incoming audio signal and sends it to the power amplifier. The power amplifier provides the electrical current necessary to drive loudspeakers.

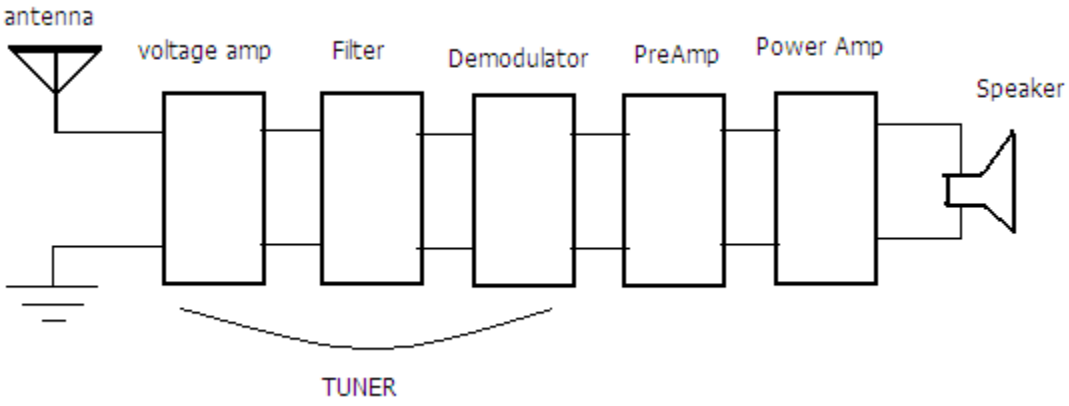


Figure 3: Block Diagram of a Radio

Non-Linear Devices

Electronic devices such as diodes and transistors have non-linear current-voltage (I-V) characteristics. The circuit elements that you have studied thus far in your circuit analysis text were linear meaning that if you plotted current vs. voltage on a graph you would obtain a straight line. For instance, an ideal voltage source has a fixed voltage that is independent of the current it produces. A resistor has a linear I-V relationship governed by Ohm's law. In contrast, a diode has a non-linear plot. The I-V characteristic plots of a voltage source, a current source, a resistor, and a diode are shown in Figure 4.

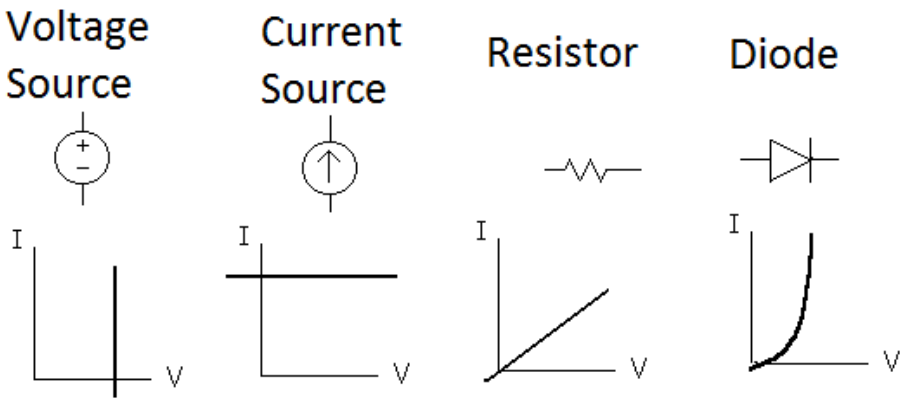


Figure 4: I-V Characteristics of Various Circuit Elements

The non-linear characteristics give electronic devices their power to process signals in a variety of interesting ways. Engineers exploit these characteristics in the design of all sorts of devices that make our life easier, safer, more interesting, and more fun.

We will learn how to analyze circuits containing electronic devices with techniques you have already learned such as KVL, KCL, and Thevenin's Theorem. We will discover that we can utilize circuit models that approximate the behavior of real electronic devices and we can then analyze the circuits using familiar circuit analysis techniques.

Conventions for Schematics and KVL used in Electronics

It is customary in the study of electronics to use a somewhat different approach to drawing schematics than what you have seen in your circuit analysis text where circuits were drawn as one or more complete loops. In this booklet and most electronic texts, circuits are typically represented with a ground and reference voltages at one or more points (See Figure 5 below). After a little practice, you will find it easy to convert from one form to another.

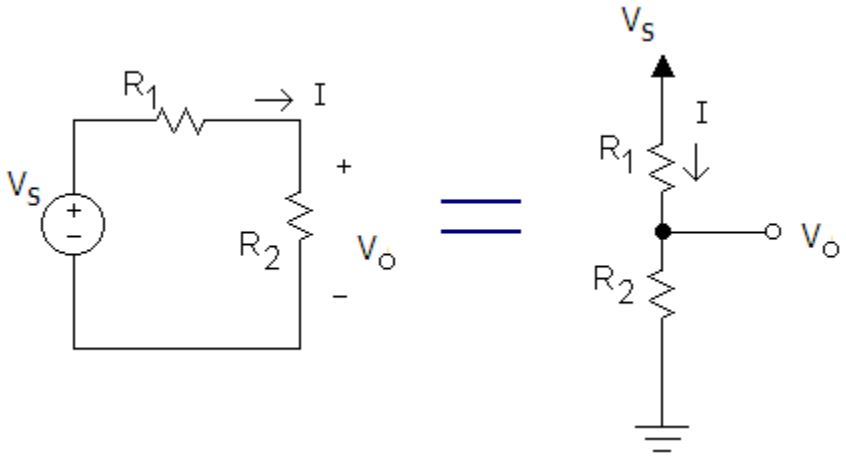


Figure 5: Schematic Conversion Example

Simulation of two circuit forms above

Sometimes you will see positive and negative voltage references in a schematic such as that shown on the left side of Figure 6. To convert, start by drawing a ground, and then create the positive and negative voltages using voltage sources as shown in the middle of the figure. The right-side schematic is simpler version of the middle schematic.

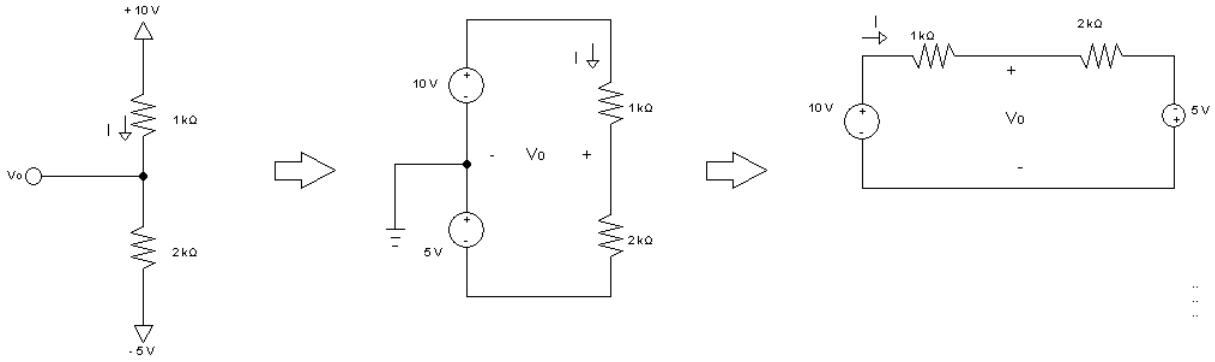


Figure 6: Schematic with Positive and Negative Voltage Sources

Simulation of Circuits Shown in Figure Above

Application of Kirchhoff's voltage law (KVL) in this booklet will be different than what you are used to. You probably have been summing voltages around a loop where a voltage rise is negative while a voltage drop is positive. In this booklet, and most other electronics texts, the convention is the opposite. The convention that is used is arbitrary; as long as you follow the rules, you will obtain the correct answer. In the circuit shown in Figure 5, we would write the following KVL equation:

$$V_S - IR_1 - IR_2 = 0$$

When writing the equation, you can think of it this way:

Start at a voltage level of Vs, we drop IR_1, we drop IR_2, and we end at ground (0V).

Simulation of More Complex Circuit

Notation for DC and Small Signals

Often electronic circuits are used for processing small AC signals such as in amplification or filtering. To process the signals, DC currents are used to "bias" or place the circuit in a certain region of operation. This will make more sense when we begin our study of diodes in the next chapter. For now, simply realize that there will often be both AC and DC voltages and currents present in a circuit. To distinguish between the two quantities, we will use the following notation:

Description	Value	Example
Upper case letter with upper case subscript.	DC - Constant	I_D=4 mA
Lower case letter with lower case subscript.	AC - signal	i_d=0.1cos10t mA
Lower case letter with an upper case subscript.	Total = DC plus signal	$i_D = I_D + i_d$ = 4+0.1cos20t mA

In the circuit show in Figure 7, the transistor is supplied with both an AC and DC voltage. The DC voltage is used to "bias" the transistor so that it can be used to amplify the AC signal. We discuss transistors in a subsequent chapter, but the transistor must be supplied with DC voltages or "biased" so that it operated in its optimal mode. In electronics, we will often have both AC and DC voltages and currents present so it is important to have a naming convention to distinguish them. In the circuit below v_a represents the signal voltage, V_A the DC voltage, and v_A the total voltage.

Simulation Showing AC, DC, and total Voltage representation

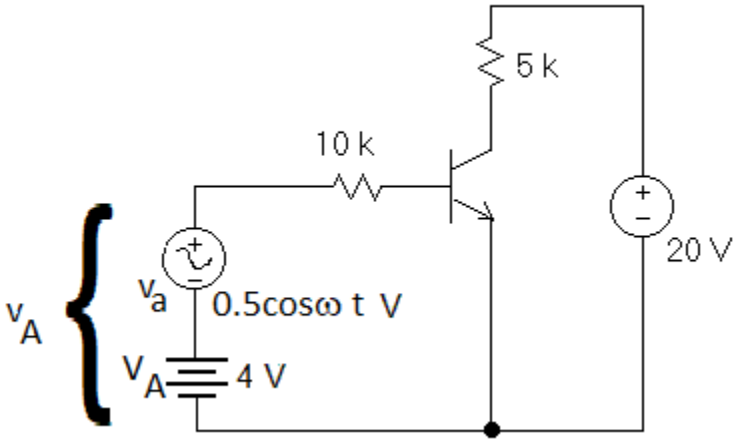
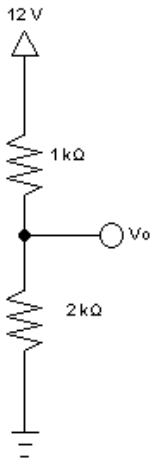


Figure 7: Amplifier Showing DC bias voltage and AC signal voltage

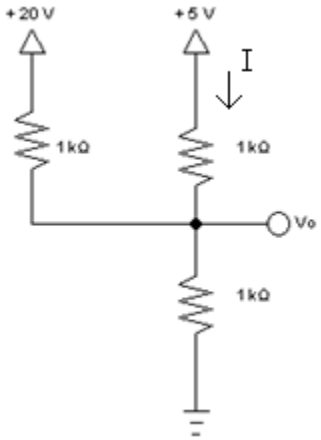
Simulation: Transistor Amplifier Circuit

Problems

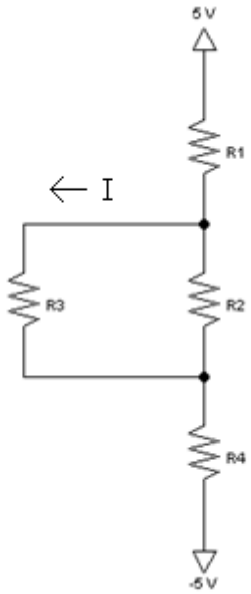
1. Redraw the circuit below so that it is in the form of a complete loop. Clearly indicate Vo on your schematic.



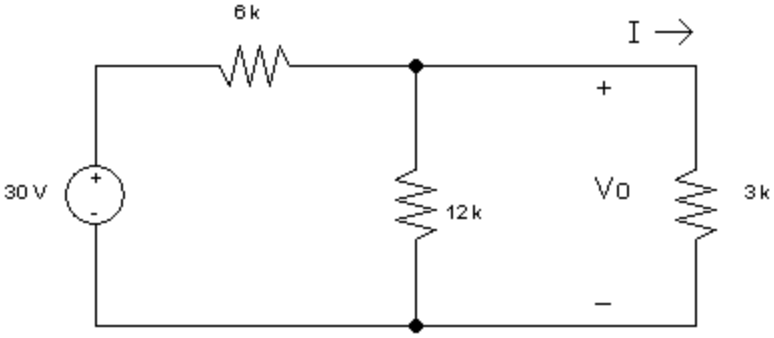
2. Redraw the circuit below so that it is in the form of complete loops. Clearly indicate Vo and I on your schematic.



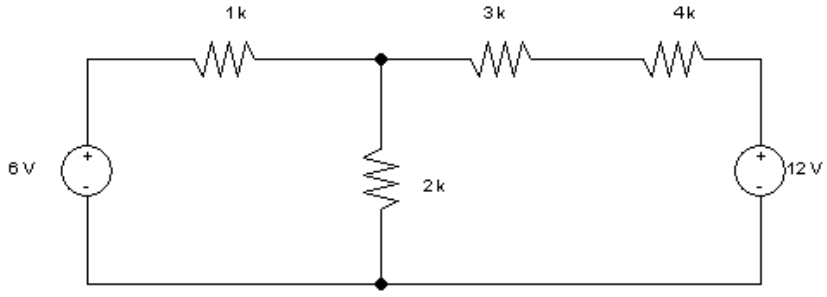
3. Redraw the circuit below so that it is in the form of complete loops. Clearly indicate I on your schematic.



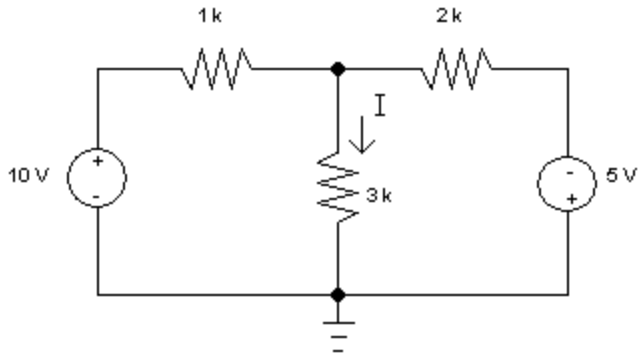
4. Redraw the circuit below so that it is in the "electronics" format. Clearly indicate Vo and I on your schematic. Take the ground reference to be at the bottom of the schematic.



5. Redraw the circuit below so that it is in the "electronics" format. Take the ground reference to be at the bottom of the schematic.



6. Redraw the circuit below so that it is in the "electronics" format. Clearly indicate I on your schematic.



7. Which of the following could <u>not</u> be true using the standard electronics convention regarding AC and DC values?
    a. $V_D = 10$ V
    b. $i_D = 3$ A
    c. $v_D = 0.2\sin\omega t$ V
    d. $I_D = 0.1\cos\omega t$ A
    e. $i_D = \{2 + 0.1\cos\omega t\}$ A

8. Determine v_D if $v_d = \{0.1\cos\omega t\}$ V and $V_D = 3$ V.

9. Draw a plot of v_D versus time if $v_d = \{0.5\cos(2\pi t)\}$ V and $V_D = 2$ V.

10. Which of the following is a legitimate expression?
    a. $I_d = 2A$
    b. $i_d = 2A$
    c. $I_D = 0.3\cos(10t)$
    d. $i_D = 2A$

11. Which of the following is a legitimate expression?
    a. $I_d = 2A$
    b. $i_d = 2A$
    c. $I_D = 0.3\cos(10t)$
    d. $i_D = 0.1\cos(20t)$

12. What variable name should be used for the current $4.0 + 0.3\cos 20t$
    a. i_d
    b. I_d
    c. I_D
    d. i_D

Chapter 2: Diodes and Diode Circuits

Introduction

Diodes are very useful yet simple devices that are found in nearly every consumer electronic product. They are especially prominent in Light Emitting Diode (LED) circuits, voltage regulators, and AC to DC power supplies. Studying diodes and diode circuits is an excellent introduction to electronic devices.

Diodes come in a variety of shapes, sizes, and electrical characteristics. Several are pictured in Figure 1.

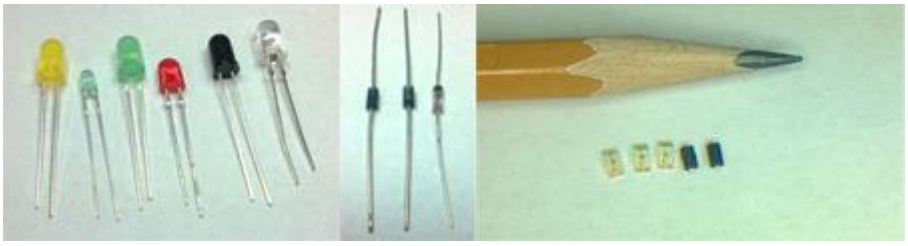


Figure 8: Photographs Various Diodes

The schematic diagrams of a common junction diode, an LED, and a Zener diode are shown in Figure 2.

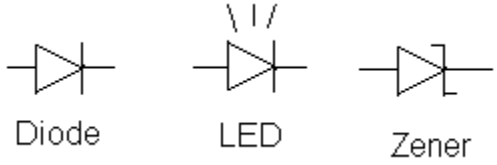


Figure 9: Schematic Symbols for Diodes

The most important characteristic of diodes are their ability to allow current to flow in one direction through them but block current flowing in the opposite direction. A mechanical analogy is the "one-way valve" known as a "check valve" (see Figure 10 below). In the check valve, fluid can flow in only one direction through the valve.

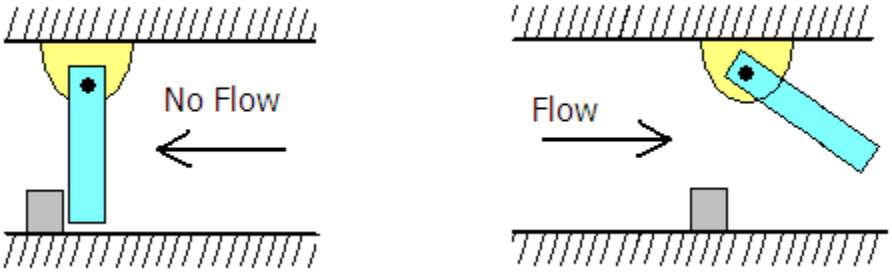


Figure 10: Check Valve Illustration

The chemical structure of the diode is responsible for its ability to pass current in one direction only. Although diode chemistry is an interesting topic, for the sake of time we will take a "black box" approach by looking at its current and voltage characteristics at its terminals. For electrical engineering students, later coursework will examine diode chemistry.

In this chapter we will examine diode properties and a variety of methods used to analyze circuits containing diodes. We begin with standard junction diode, followed by a brief look at LEDs, and then an examination of zener diodes. Next we introduce a methodology called small signal analysis which we will find extremely useful later when analyzing transistor based circuits. We end the chapter with a look at AC to DC conversion using diodes.

Simulation

Simulation is a powerful tool that can be used to predict the behavior of a circuit prior to construction. It can also be used as a design tool that allows the engineer to quickly test different designs. Simulation is not a replacement for understanding how to analyze circuits as understanding how to analyze diodes leads to a better understanding of how to design diode circuits.

There are many simulation tools available for simulating electronic circuits. PSpice is the industry standard and offers powerful tools that produce accurate results. A simulation tool that will be used in this chapter and throughout the remainder of the book is the Java Circuit Simulator – an online simulator that is easy to use and is a great learning tool because it produces an excellent visual representation of circuit operation.

Result from simulation may not match hand calculations. This is to be expected because the underling mathematical model used in the simulator may be different from the one you use for calculation. Typically the results from simulation will better match real circuit behavior because the mathematical models used by the simulator are more sophisticated. Consequently, do not be surprised to see that your calculated circuit parameters are not exactly the same as produced by the simulator. You are strongly encouraged to look at each of the simulations that integrated into the text as they should provide you with insight in how electronic circuits work.

Junction Diodes

Junction diodes (so named because of the p-n junction responsible for its characteristics) are the most common type of diodes and are used in many different applications. The fundamental concepts that you learn regarding junction diodes behavior are applicable to other types of diodes as well.

In order to better understand the junction diode, we examine its current versus voltage (I-V) relationship at its external terminals by means of a simple experiment. We construct the circuit shown in Figure 11 below and vary the voltage source, V_S, and measure the current and voltage for the diode at various voltage levels. If we plot the corresponding points on a graph we would get a result similar to that shown in Figure 12.

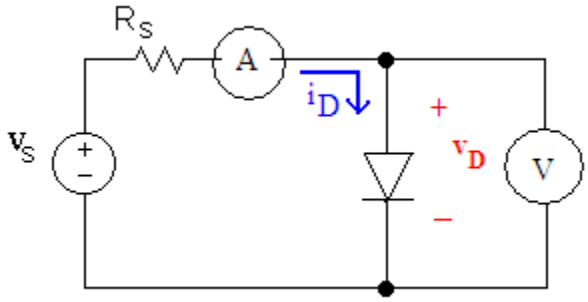


Figure 11: Circuit to Illustrate I-V Characteristic of a Junction Diode

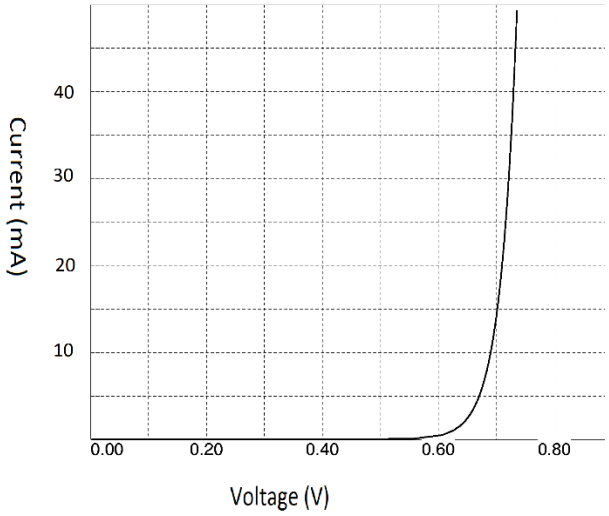


Figure 12: Diode I-V Characteristic Curve

You may be wondering why we don't simply eliminate resistor R_S and put the voltage source (Vs) directly across the diode. The problem is that it would be very easy to overload our voltage supply or destroy the diode because the diode passes current freely beyond about 0.7 volts.

From the graph, we see that almost no current flows through the diode until the diode voltage for voltages less than 0.5 volts. After the diode voltage reaches about 0.7 V current flows quite freely.

Simulation: I-V Characteristics of a Diode

It is evident from the I-V graph in Figure 12 that the diode is a non-linear device; that is its I-V relationship is not a straight line. This is in contrast to all the circuit elements you have studied thus far in your circuit analysis text. The I-V characteristic plots of a voltage source, a current source, a resistor, and a diode are shown in Figure 4.

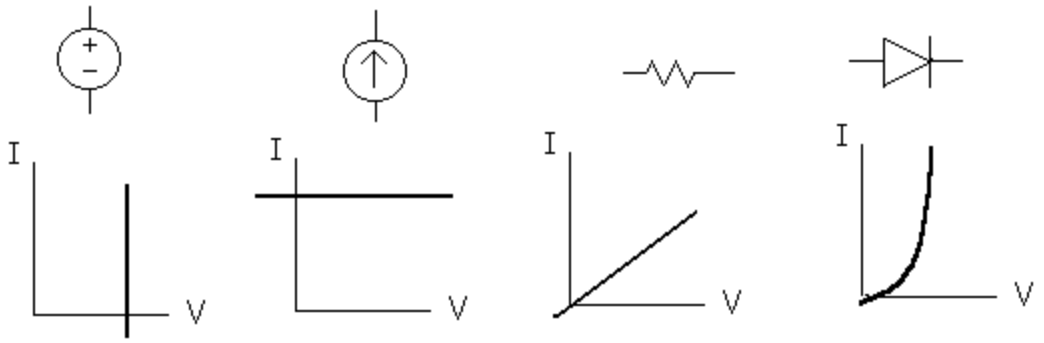


Figure 13: I-V Characteristics of Various Circuit Elements

Analyzing circuits containing non-linear devices is both more difficult and more interesting than what you have studied thus far. The challenge is to devise strategies that we can use to analyze and design circuits that contain diodes. In later chapters, we will see that similar strategies can be applied to transistor based circuits.

Modeling Techniques

We will learn a variety of strategies to analyze circuits containing diodes that vary in complexity and accuracy. The strategies that we will examine include a graphical approach and several modeling approaches. We will begin with the simplest model called the "ideal diode" model.

Ideal Diode Model

If we were to plot the behavior of an "ideal diode", i.e. one that allows current flow freely in one direction but blocks the current from flowing in the opposite direction, it would have the I-V characteristic shown in Figure 14. This graph shows that the current can flow freely and that there is no voltage drop when the current is flowing forward through the diode. However, no current flows "backward" through the diode no matter what the voltage is. When current is flowing through the diode we call the diode "forward biased" and when no current flows we call this state "reverse bias". We also refer to these states as the diode being "on" or "off" respectively.
So how should we model these states? If the diode is forward biased or "on", there is no voltage drop across the diode, thus a **short circuit** can be used to model this state as there is no resistance. If the diode is reverse biased or "off", there is no current flow and we can model this state as an **open circuit**. See Figure 15 for representations of these models.

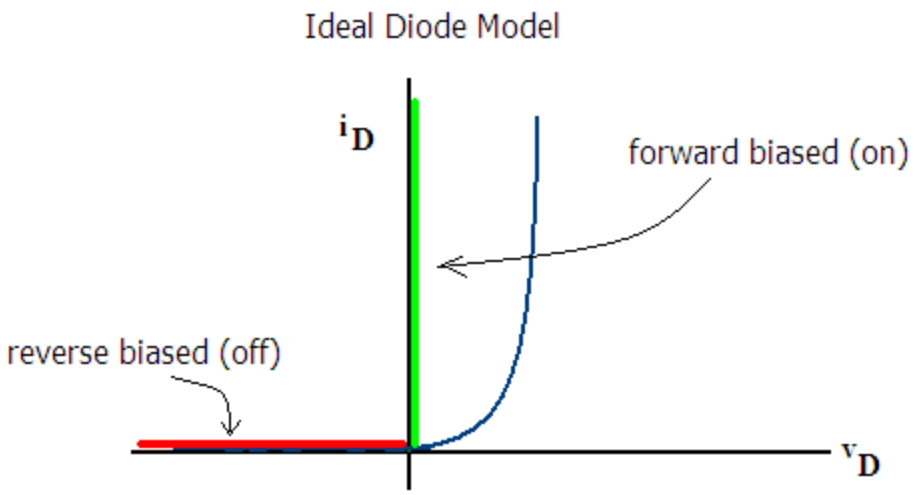


Figure 14: Ideal Diode I-V Characteristic

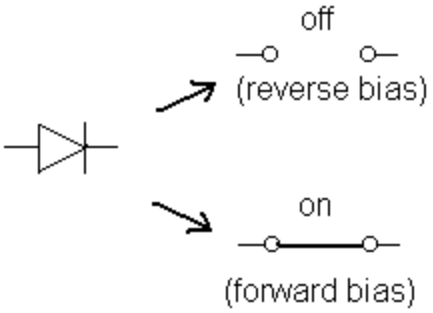
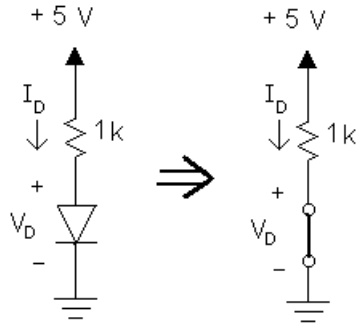


Figure 15: Ideal Diode Models

How do we know if a diode will be forward or reverse biased? The answer is that we can often determine its state by inspection but in those cases that we can't, we can assume a state, analyze the circuit and then verify that our assumption was correct. If our assumption was incorrect, we must reanalyze the circuit with a different assumption regarding the state of the diode. For instance if we assume a diode is forward biased and when we analyze the circuit it turns out to be reverse biased, then our assumption of forward biased is incorrect and we need to use our reverse bias model of an open circuit and re-analyze the circuit.

Example 1: Simple Diode Problem using Ideal Diode Model

Use the ideal diode model to determine the current I_D and voltage V_D in the following circuit. By inspection, it appears the diode will be in the ON state. Consequently, we will replace the diode with the forward biased short circuit model.



KVL yields:

$$5 - (1k)i_D = 0$$

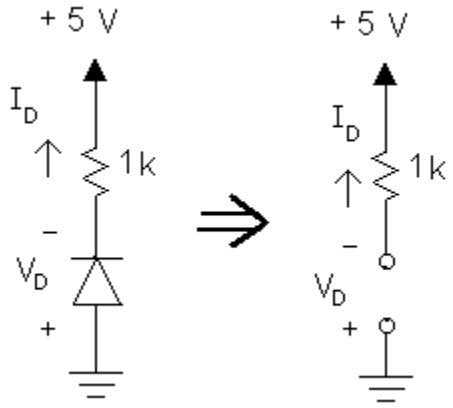
$$i_D = 5.0\,mA$$

Note that the current passes through the diode in the forward direction so our assumption of the diode being forward biased was correct. If the current were negative that would violate the assumption that we made that the diode was on.

Simulation: Diodes in Forward and Reverse Bias

Example 2: Diode in Reverse Bias

Now we will analyze the same circuit except the diode orientation has been reversed.



For this circuit, the diode appears to be reverse biased so we replace the diode with the open circuit model. By inspection, we see that the diode current is zero.

KVL yields:

$$5 + (1k)0 + V_D = 0$$

V_D= -5 V and I_D = 0

Note that the voltage V_D is less than zero so our assumption of reverse bias has been verified.

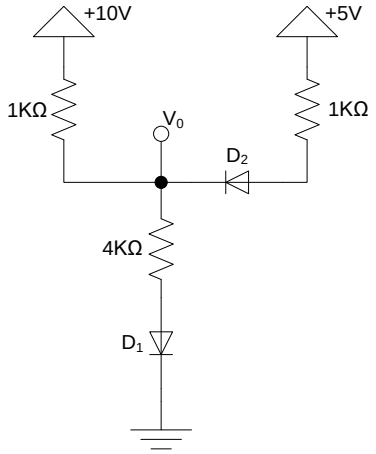
To summarize, the steps of the analysis strategy are:

1. Assume a state for the diode.
2. Substitute the appropriate model (replacing the diode with either an open circuit or short circuit).
3. Analyze the circuit. Calculate the current through diodes that were assumed to be "on" and voltages across diodes that were assumed to be "off".
4. Verify assumptions. Ensure diodes that were assumed to be on have current flowing in the correct direction. Also, verify that reverse biased diodes have the correct polarity.
5. If any assumptions were incorrect, make new assumptions and reanalyze the circuit.

We will now turn our attention to a more difficult circuit containing multiple diodes where it is not as obvious which states the diodes will be in.

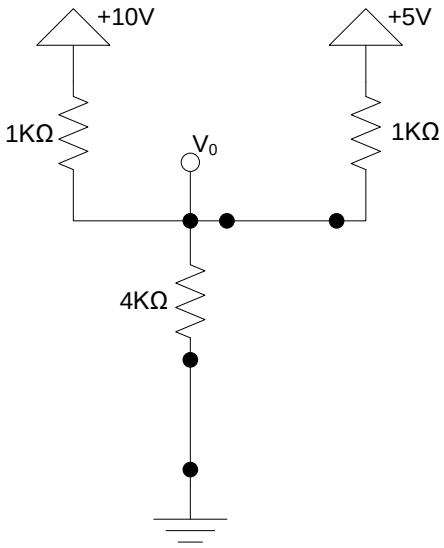
Example 3: Multiple Diode Circuit

Determine the voltage Vo (measured with respect to ground) in the circuit below.

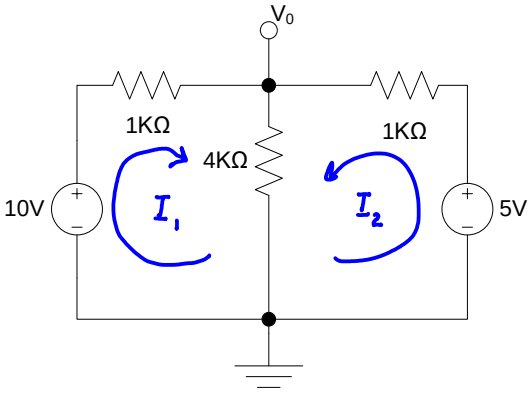


Can you guess the state of each diode in the circuit above? The 10 V source should cause current to flow toward ground so we guess that D_1 is on. It is a bit harder to determine the state of D_2.

To analyze this circuit we must first assume states for each of the diodes. To begin, let's assume that both diodes are "on". Replacing D_1 and D_2 with short circuits yields the circuit below.



If we wish, we can redraw the circuit to make in the more familiar style of the circuits you have analyzed in your circuit analysis text.



Using mesh analysis yields the following equations:

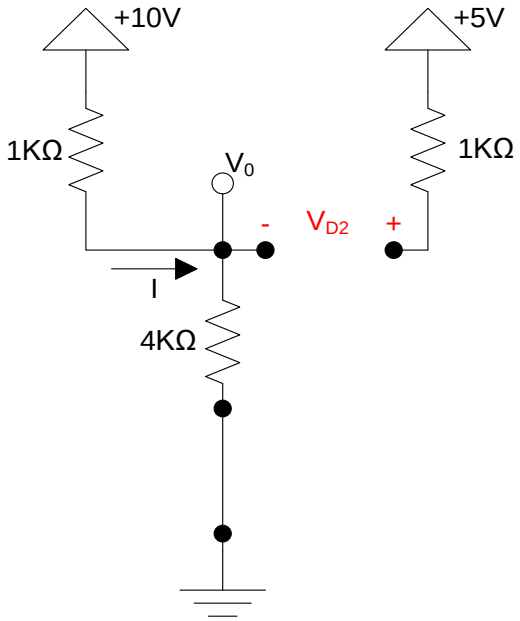
$$Left\ Mesh\text{:}\ 10 - 1k(I_1) - 4k(I_1 + I_2) = 0$$

$$Right\ Mesh\text{:}\ 5 - 4k(I_1 + I_2) - 1k(I_2) = 0$$

Solving yields I_1 = 3.33 mA, I_2 = -1.67 mA

Now we examine these results with respect to our initial assumption of both diodes being on. For diode D_1 the current is I_1+I_2 which is 1.67 mA downward through the diode in the forward bias direction and consequently our assumption is correct for this diode. For diode D_2 the current I_2 is negative which reverse biases this diode so our assumption for this diode is incorrect.

Since the assumed state for one of our diodes is incorrect we must re-analyze the circuit using a different set of assumptions regarding the states of the diodes. Since our assumed state for D_1 was correct we will maintain our assumption that it was "on" but for diode D_2 we will now assume that diode is "off". The circuit below shows the circuit with the appropriate models substituted for D_1 and D_2.



A single KVL equation can be used to solve this circuit.

$$10 - 1k(I) - 4k(I) = 0$$

I =2 mA.

The current I is positive which verifies our assumption that D_1 is "on". Let's examine the state of diode D_2 to verify that it is reverse biased. The voltage V_{D2} can be found by KVL:

$$V_{D2} = 5 - V_O = 5 - 4k(I)$$

V_{D2} = -3 V

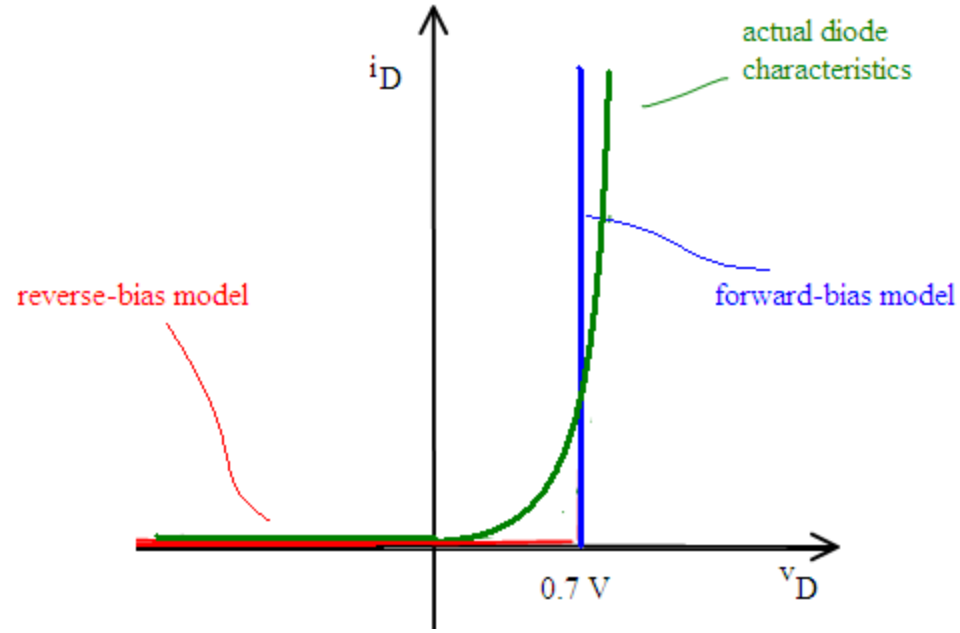
This voltage does indeed reverse bias the diode which verifies our assumption.

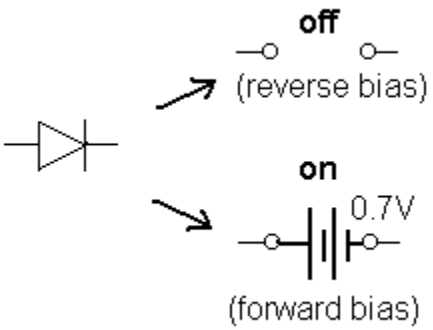
Simulation: Circuit with Two Diodes Modeled with Switches

Simulation: Circuit with Adjustable Resistance and Two Diodes

The Constant Voltage Drop Model

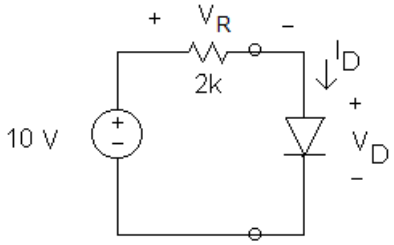
The constant voltage drop model is similar to the ideal model except that when the diode is forward biased we represent the diode as causing a fixed voltage drop. For a common silicon junction diode a voltage of 0.7 V is typically used. Although not quite as simple as the ideal model, results are more accurate.





Example 4: Using the Constant Voltage Drop Model

Determine the diode voltage and current for the circuit below using the constant voltage drop model.



For this circuit, it appears as though the diode will be forward biased. We can replace the diode with its forward biased constant voltage drop model. By inspection we can determine that the voltage across the resistor is 9.3 V and therefore the current I_D is 4.65 mA. Since the current is

going through the diode in the forward direction we have verified that our assumption is correct. Compare this to the ideal diode model, which is more accurate?

The constant voltage drop model is more accurate because it more closely resembles the actual I-V characteristics of the diode.

If you assume a diode is reverse biased with the constant voltage drop model, how do you determine whether it is indeed reverse biased?

The diode voltage must be less than 0.7 V.

The constant voltage drop model is not quite as easy to use as the ideal diode model however the results are more accurate. For greater accuracy, we can use the exponential model or graphical techniques. We begin with graphical techniques.

Load Line Analysis

Load line analysis is a graphical technique used to find the current and voltage of a diode. Although more time consuming than the other techniques discussed thus far, it provides helpful qualitative insights regarding circuit behavior such as how circuit parameters impact the behavior of the circuit. In load line analysis we graph the I-V characteristics of the diode on the same diagram of the I-V characteristics of the energizing circuit (the load line). The intersection of the two plots represents the operating point (also known as the quiescent point or Q-point) of the circuit which we shall denote as V_{DQ}, I_{DQ} (see Figure 16)

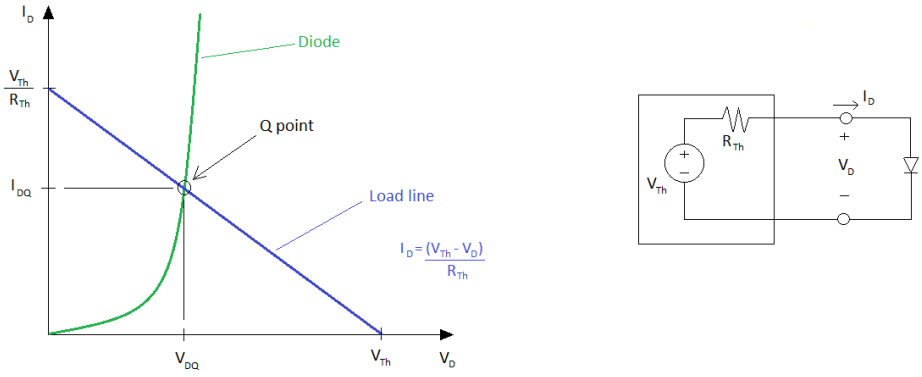


Figure 16: Load Line Analysis

In the figure above, the linear circuit attached to the diode has been reduced to its Thevenin equivalent. The load line equation can be found by using a KVL equation of the circuit:

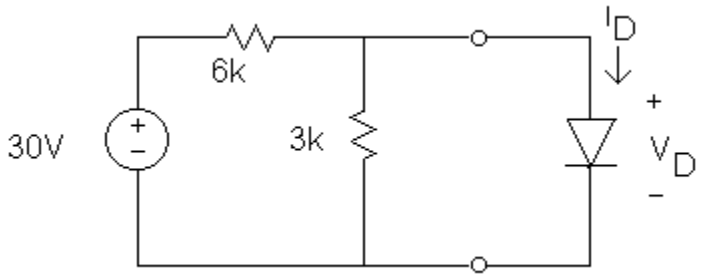
$$V_D = V_{Th} - I_D R_{Th}$$

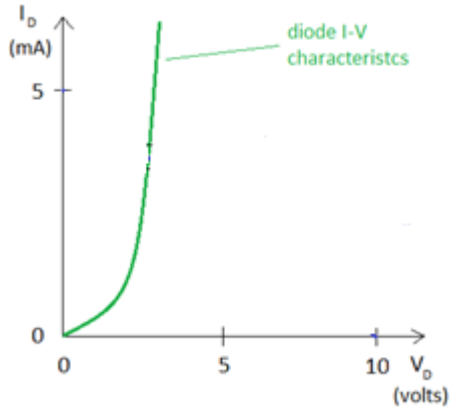
Therefore: $$I_D = \frac{V_{Th} - V_D}{R_{Th}}$$

The I-V characteristics of the diode can be obtained from a data sheet for the diode (or by plotting the Shockley equation which we discuss in the next section).

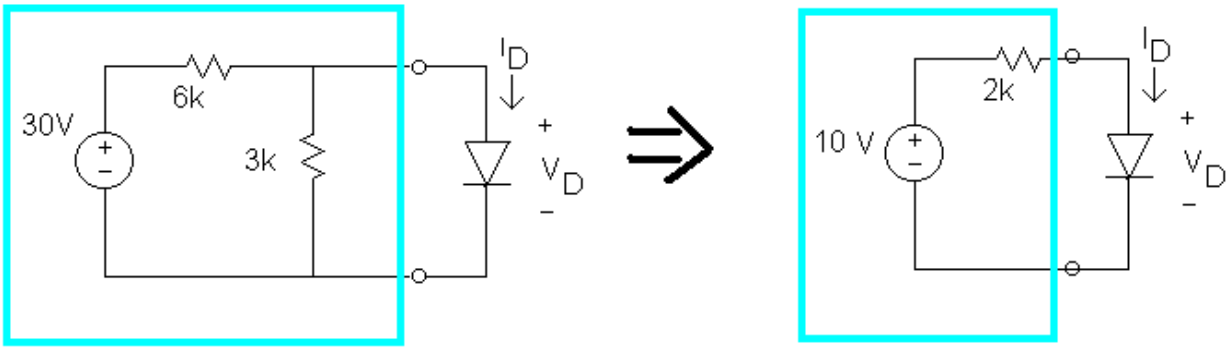
Example 5: Load Line Analysis

Find the operating point of the circuit below using load line analysis. Assume the I-V characteristic of the diode is that shown below.

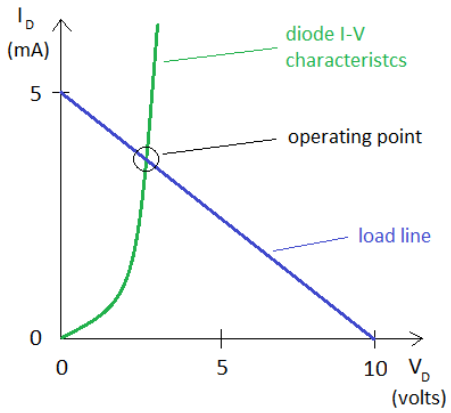




From Thevenin's theorem, we know that a linear circuit can be reduced to a voltage source in series with a resistor. For the circuit attached to the diode, the open circuit voltage is 10 V. Replacing the independent voltage source with a short circuit and finding the resistance at the terminals gives a Thevenin resistance of 2 kΩ.



We are now ready to construct the load line of the Thevenin equivalent of the circuit attached to the diode. We need to establish 2 points on the line, the easiest being when the circuit is attached to an open circuit and short circuit. The open circuit condition will give 10 V at 0 A. The short circuit condition results in a voltage of 0 V and current of 5 mA. We plot these 2 points and connect them with a straight line as shown in the figure below.



The intersection of the load line with the diode I-V characteristics reveals the operating point which is approximately V_D = 2 V and I_D = 4 mA. This diode is probably not a junction diode since its turn on voltage is much higher than we would expect for a standard junction diode (0.7 V typically). Perhaps this is an LED – which we discuss in the next section.

When constructing the load line, sometimes you may want to choose other points on the graph besides open and short circuits depending on the scale of your graph. Any two points will work, for example we could choose V_D = 5 V. Using Ohm's Law I_D, can be determined:

$$I_D = (10 - 5)/2 \; = \; 2.5\, mA$$

This point is then joined with point I_D=5 mA at V_D= 0 V resulting in the same load line as above.

Examine the load line in the problem above. If we wanted to reduce the current, how might we alter V_{Th} and/or R_{Th}? What effect does increasing V_{Th} have on the slope of the graph? What effect does increasing R_{Th} have on the slope of the graph?

To reduce current we can either decrease V_{Th} or increase R_{Th}.
Increasing Vth has no effect on the slope of the load line.
The slope of the load line becomes more horizontal.

Exponential Model - The Shockley Equation

An exponential equation that closely approximates the I-V characteristics of diodes is the Shockley Equation:

$$i_D = I_S(e^{v_D/V_T} - 1)$$

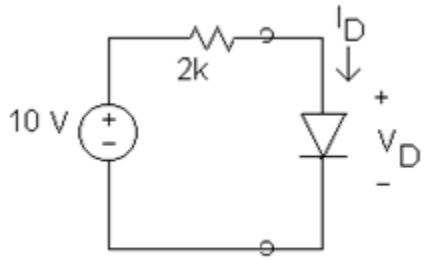
The constant I_S is called the saturation current and is typically on the order of 10^{-15} A. The constant V_T is the thermal voltage and is approximately 25 mV at room temperature.

Examining the Shockley equation reveals that if i_D is not very small, the first term in the brackets must be much larger than 1. Therefore, for diode currents that are not extremely small, a good approximation can be obtained using the simplified version of the Shockley equation:

$$i_D = I_S(e^{v_D/V_T})$$

Example 6: Shockley Equation

Use the Shockley equation to solve for the diode current in the circuit below.



The Shockley equation provides an equation relating diode current and voltage. This equation contains two unknowns. Using Ohm's law we can write the second equation necessary to solve for the two circuit parameters.

$$i_D = \frac{10 - v_D}{2k}$$

Substituting $I_S=10^{-15}$ A and $V_T = 25$ mV into the simplified Shockley equation yields:

$$i_D = 10^{-15}(e^{v_D/0.025})$$

We have a linear equation and one non-linear equation that relate the two circuit parameters i_D and v_D. We can solve these equations using a graphing calculator by plotting these equations and finding the operating point as we did in load line analysis.

Alternately, we can equate the equations above and either calculate directly using a calculator or use iteration (guess a value for v_D, calculate the result, and guess again). An initial guess of v_D = 0.7 V would be an excellent initial guess don't you think?

$$10^{-15}\left(e^{v_D/0.025}\right) = \frac{10 - v_D}{2k}$$

Diode Application: The Rectifier Circuit

A rectifier is used in the AC to DC conversion applications. The power supply that you plug into the wall to charge your cell phone battery typically has a rectifier. There are two different types of rectifiers; the "half wave" and the "full wave" rectifier. We begin with the half wave rectifier before turning our attention to the full wave rectifier.

Half Wave Rectifier

The circuit shown in Figure 17 is called a "half wave" rectifier because its output is the positive half of the input waveform. When $v_{in}(t)$ is positive, the diode is forward biased (think short circuit) and v_{out} is equal to v_{in}. When $v_{in}(t)$ is negative, the diode is reversed biased blocking the current and hence the voltage across R_L is zero during this interval of time. The resulting output waveform is shown in Figure 18. The output voltage peak will be about 0.7 volts less than the input peak because of the voltage drop across the diode.

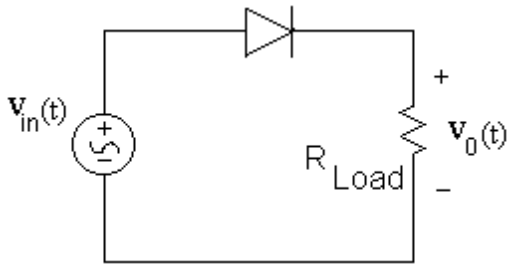


Figure 17: Half Wave Rectifier

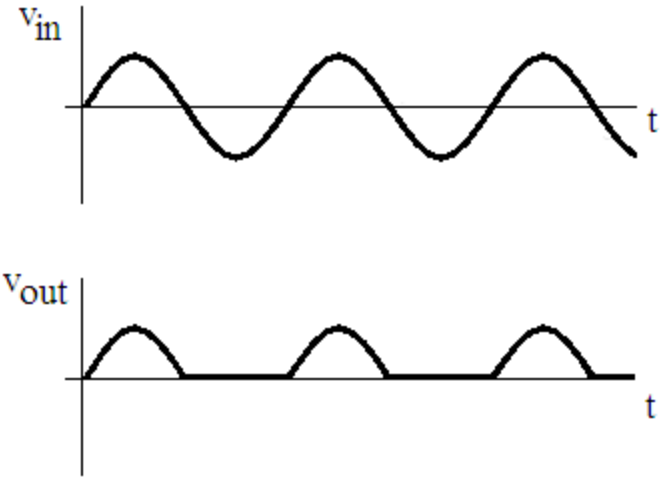


Figure 18: Half Wave Rectifier Input/Output Waveforms

Simulation: Half Wave Rectifier

Full wave rectifier

A “full wave" rectifier is shown in Figure 19. The 4 diodes comprising the "diode bridge" direct the current from left to right no matter whether the input voltage polarity is positive or negative. The output waveform is shown in Figure 20. The output voltage peak will be about 1.4 V less that the input peak. Why?

Because 1.4 volts are dropped across the 2 diodes that are currently on.

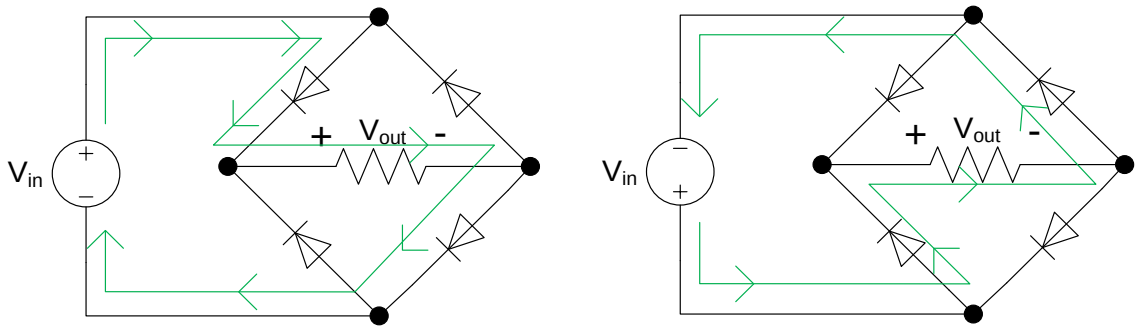


Figure 19: Full Wave Rectifier

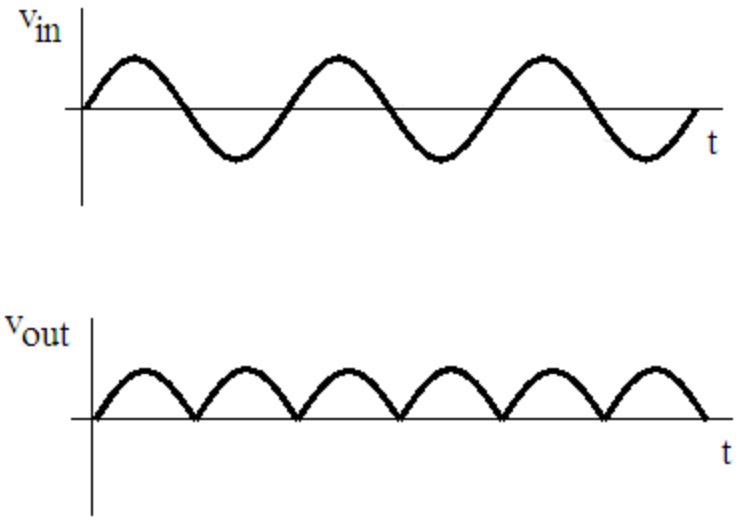


Figure 20: Full Wave Rectifier Input/Output Waveforms

Simulation: Full Wave Rectifier

Light Emitting Diodes

So far we have focused our attention on the most common type of diode, the junction diode. Now we will examine two other diode types, the light emitting diode (LED) and the zener diode. We begin with the LED.

LED behavior is similar to the junction diode except that the turn on voltage is higher. Of course the most important aspect of the LED is that it emits light when current passes through it. LEDs are much more efficient than standard incandescent light bulbs which is the main reason for their increasing popularity. Another advantage of LEDs is that they last much longer than standard bulbs. The "turn on" voltage for LEDs varies depending on the how the LED is manufactured and the color of the LED and is typically on the order of 1.5-3.5 V. LEDs can be destroyed if too much current passes through them so it's important to heed the guidelines provided in the manufacturer's data sheet.

To analyze a circuit with an LED or multiple LEDs the best method to use is the constant voltage drop model. The ideal diode model is not as accurate since the turn on voltage for LEDs is considerably higher than that of standard junction diodes.

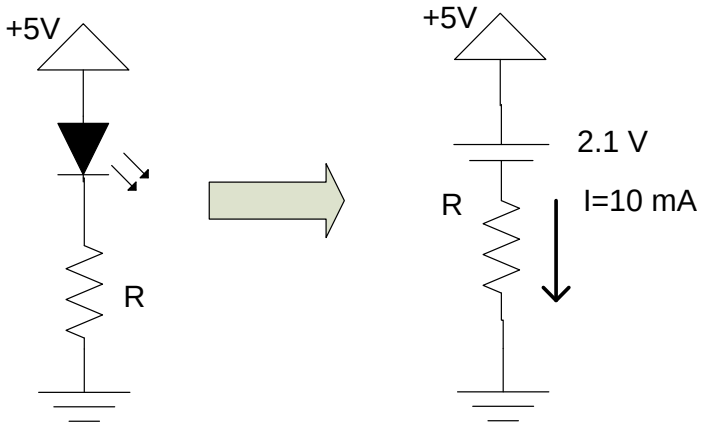
Example 7: LED Circuit

Design a circuit to turn on an LED using the output pin of a microcontroller. Assume the turn on voltage of the LED is 2.1V.

Scenario: A microcontroller is used to turn on and off an LED. The microcontroller output can be set either high or low (5V or 0 V). When the LED is on, we would like limit the current flow

to approximately 10 mA because too much current will destroy the LED. We can place a resistor in series with the LED to limit current.

We start by creating the circuit model shown on the left side of the figure below. Because the LED will be on, we model the LED with a voltage source (using the constant voltage drop model) as shown on the right. Note that we have assigned a current of 10 mA which is our design objective. The only unknown is the resistor value.



Using KVL we can see that the voltage across the resistor is 5 - 2.1 = 2.9 V. The resistor required to limit the current to 10 mA can be determined using Ohm's law.

$$R = \frac{V}{I} = \frac{2.9}{10\ m} = 290\ ohms$$

Simulation: Circuit with LEDs

Zener Diodes

When a negative voltage is placed across a diode and is gradually increased, the diode will enter the "reverse breakdown" region and it will begin to pass current as it does in the forward bias region. This "breakdown" voltage is something to be avoided in standard junction diodes and is given by the Peak Inverse Voltage (PIV). The zener diode is a special type of diode designed to operate in the reverse breakdown region without damage. You can purchase zener diodes with specific breakdown voltages to suit a variety of applications.

Zener Diode Characteristics

The I-V characteristics of a zener diode are shown in Figure 21. For positive voltages, the zener acts much like a junction diode. For negative voltages, we see that the diode breaks down at a particular voltage and passes current freely beyond this voltage. This property if very useful for regulator circuits which will examine in the next section. To analyze zener diode circuits the constant voltage drop model can be used where we replace the zener with a voltage source equal to its breakdown voltage when the diode is biased in the reverse breakdown region. Under forward bias conditions, either the ideal model or constant voltage drop model is generally used. Of course, we use an open circuit if the zener is operating between these modes. When analyzing

a circuit with a zener diode, you will assume the state the diode is in, and then check the assumption, as was done previously with junction diodes.

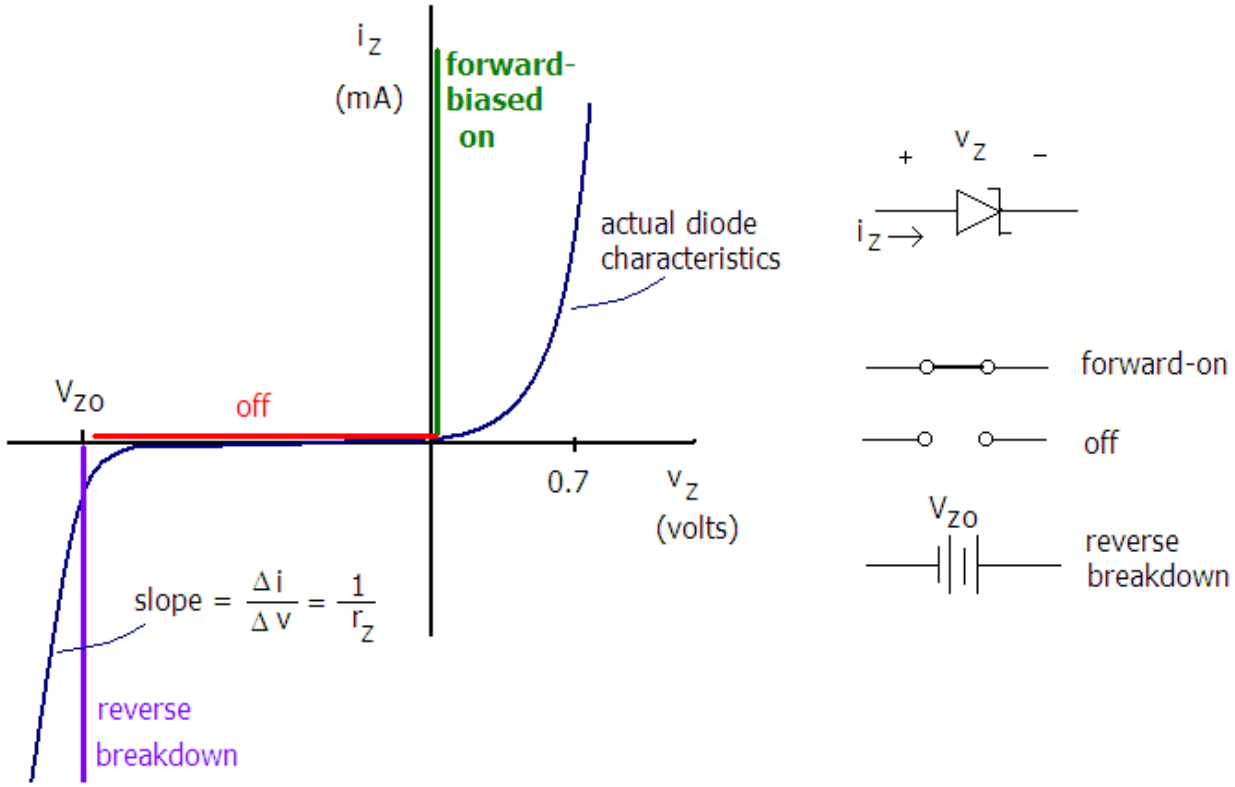
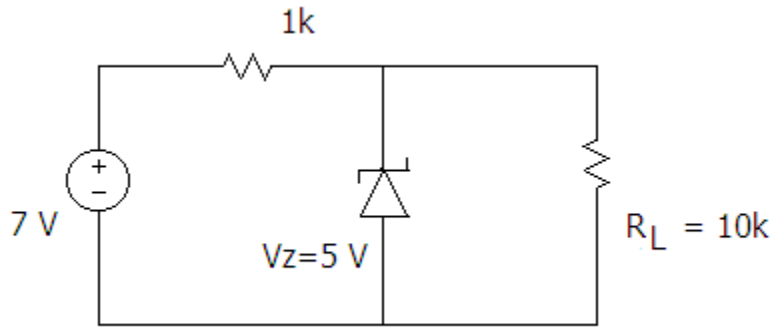


Figure 21: Zener Diode I-V Characteristic Curve and Models

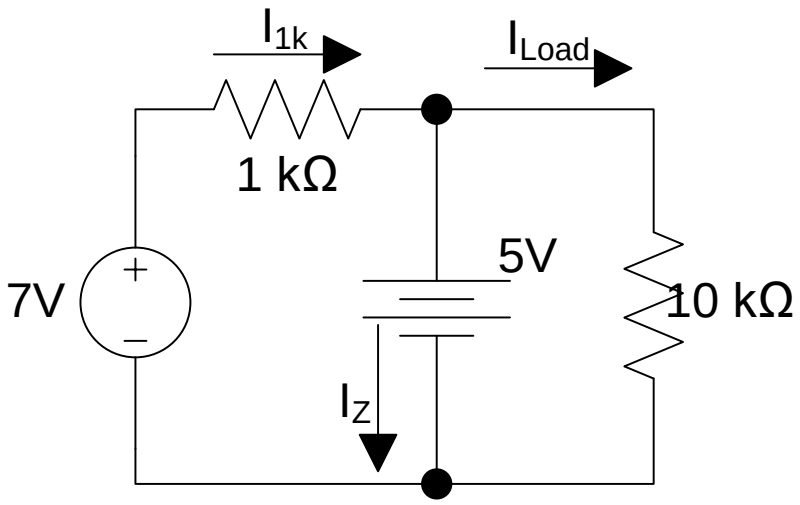
[Simulation: I-V Characteristics of a Zener Diode]

Example 8: Zener Diode Circuit

Determine the voltage across the resistor R_L, and the current through the 1 kΩ resistor. Assume that the zener breakdown voltage V_{ZO} = 5 V.



It appears that the zener is biased in the reverse breakdown region so we replace the zener with a 5 V source. We do this because the zener will have a voltage drop of approximately 5V if it is biased in the reverse breakdown region.



The voltage across the 10 kΩ resistor is obviously 5 V. Using Ohm's Law we find the currents I_{Load} and I_{1k}.

$$I_{Load} = \frac{V_{Load}}{R} = \frac{5}{10k} = 0.5\ mA$$

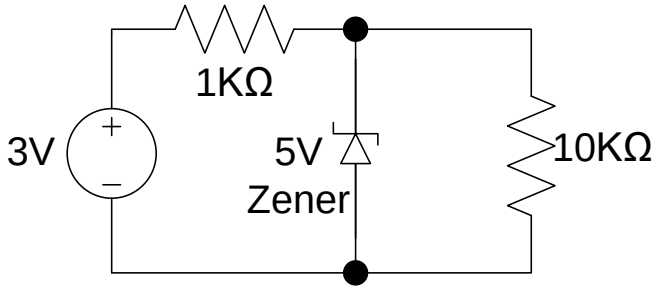
$$I_{1k} = \frac{V_{source} - Vz}{R} = \frac{(7-5)}{1k} = 2.0\ mA$$

The current I_Z is determined from KCL:

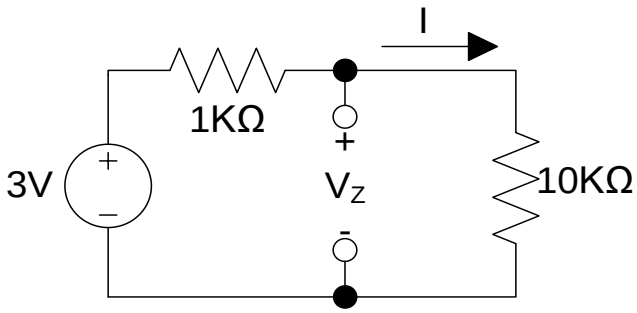
$$I_Z = I_{1k} - I_{Load} = 2.0 - 0.5 = 1.5\ mA$$

The current I_Z is referenced downward through the diode in the reverse biased direction and therefore our assumption is verified.

Example 9: Zener Diode in Cutoff



This circuit is identical to the previous example except that the voltage source is 3 V. If we were to assume the reverse breakdown region we would obtain a current upward through the diode which violates our assumption. By inspection it appears that the diode is in the off region. Under this assumption we draw the following circuit model.



The current through this single loop circuit is:

$$I = \frac{V}{R} = \frac{3}{1k + 10k} = 0.273\ mA$$

We can verify our assumption that the zener diode is "off" by determining the voltage V_Z. Using Ohm's Law find that Vz= IR = (0.273mA)(10k) = 2.73 V.

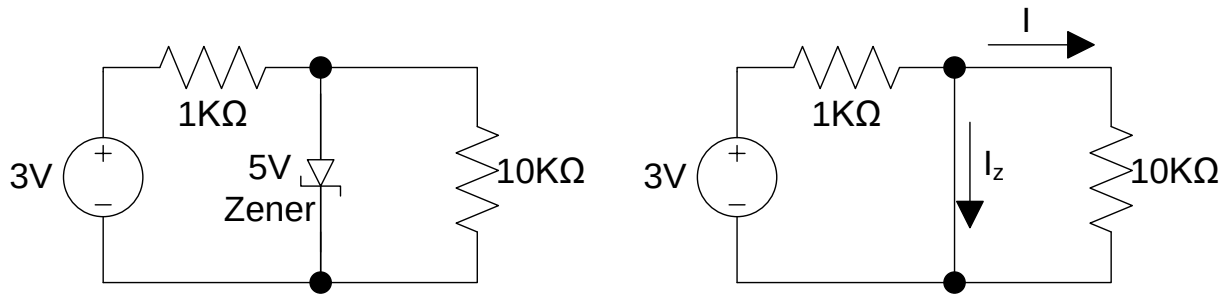
This voltage negatively biases the zener but does not exceed the breakdown voltage. Therefore our assumption is correct.

5 > Vz > 0. Assumption verified.

Simulation: Zener Diode in Reverse Breakdown and Cutoff

Example 10: Zener Diode in Forward Bias

In the circuit below, the zener appears to be forward biased. We can use either the ideal or constant voltage drop models. Using the ideal diode model, we draw the circuit as shown.



Analyzing this circuit yields:

$$I_Z = \frac{3}{1k} = 3\ mA$$

Note that the current is in the forward biased direction so our assumption is verified.

Zener Diode Applications

Next we examine two zener diode applications; the clipper circuit and the voltage regulator. We begin with clipper circuits.

Clipper Circuits

Clipper circuits use zener diodes to clip off the top and/or bottom of an input voltage waveform.

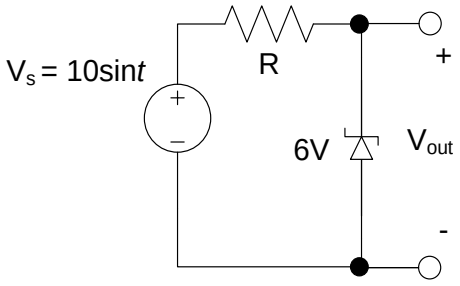


Figure 22: Simple Clipper Circuit

In Figure 22 the voltage input V_S is a sine wave with an amplitude of 10 V. As the voltage output from the source goes from 0 V to 6 V, the zener diode will be "off", no current will flow through the circuit, and consequently there will be no voltage drop across R. With no voltage drop across R, the output voltage will be equal to that of the input waveform. As V_S becomes greater than 6V, the zener diode will be in reverse breakdown and the output voltage will remain fixed at 6V. When the zener is reverse breakdown, current will flow through the circuit and the resistor drops the remaining voltage between Vs and Vout. As the input voltage drops below 6 V, the zener will again be "off" and the output voltage will track the input voltage since no current flows through the circuit. Once the input voltage becomes negative, the zener will be forward biased

and the output voltage will be zero (using the ideal model) or 0.7 V (using the more accurate constant voltage drop model).

Figure 23 shows the output of the clipper as a function of time. Another way to illustrate the properties of a clipper circuit is using a plot where the output voltage is plotted as a function of the input voltage as shown in Figure 24. Such a graph, known as the transfer characteristic, illustrates how a circuit transforms or processes an input signal.

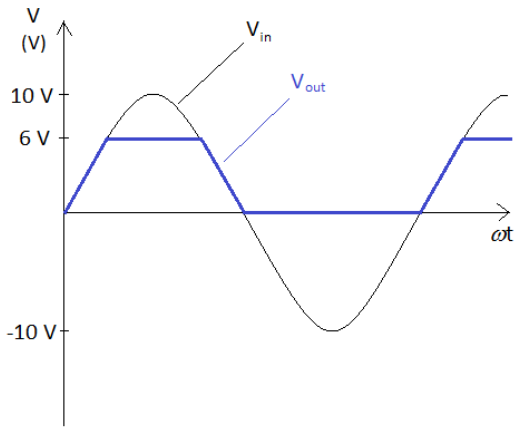


Figure 23: Clipper Circuit Input/Output Waveforms

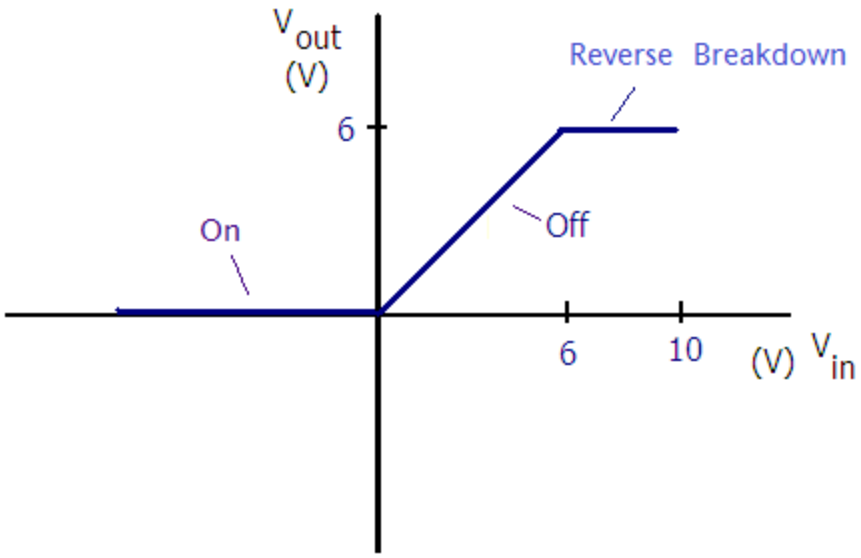
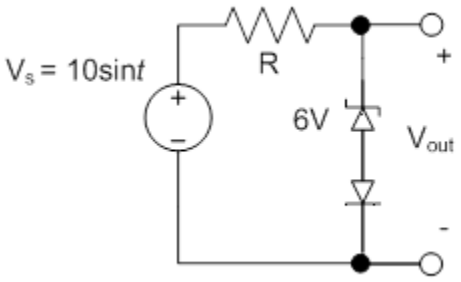


Figure 24: Transfer Characteristics of a Clipper Circuit with One Diode

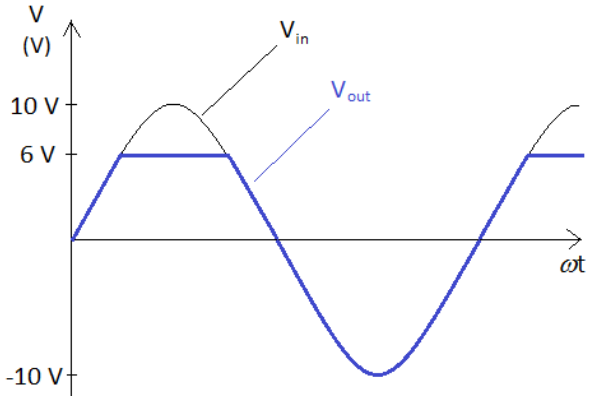
Simulation: Simple Clipper Circuit

Example 11: Clipper Circuit

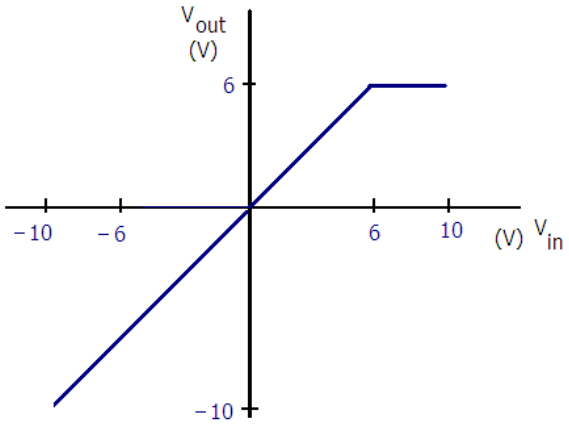
For the circuit below, plot the output voltage as a function of time. Also plot the transfer characteristics for this circuit.



The circuit is the similar to the one in the previous example except a junction diode has been added. The junction diode blocks current during the negative portion of the input waveform so that the output voltage tracks the input voltage for negative voltages as shown in the v_{out} vs. time graph below.



From the graph above, we can plot the transfer characteristics as shown below.

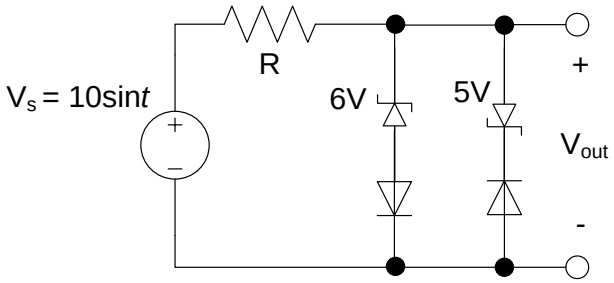


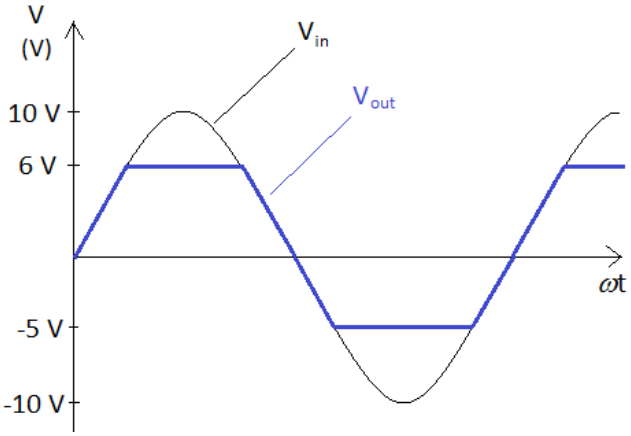
Simulation: Clipper Circuit – Top Clipped Only

Simulation: Clipper with a Switch

Example 12: Another Clipper Circuit

Analyze the clipper circuit below to determine the output voltage waveform.





This circuit behaves the same as the circuit in the previous example except during the negative cycle of the sine wave. For negative voltages, the output will track the input voltage until the input voltage is between -5 V and -10 V. During this interval, the 5 V zener will be in reverse breakdown resulting in the input waveform being clipped at -5 V.

Simulation: Clipper –Both Top and Bottom Clipped

What would happen if the junction diodes are eliminated from the circuit?

The output voltage will be zero since the zener diodes alternately pass current.

Can you figure out a way to eliminate the junction diodes from the circuit and get the same results?

Put the zeners in a back to back series configuration.

Zener Diodes in Voltage Regulators

A voltage regulator is a circuit that provides stable output voltage despite changes in the source voltage or load resistance. They are used in the last step of AC to DC conversion in a power supply. Zener diodes can be used as a "shunt regulator" to provide a relatively stable DC voltage to a load despite changes in source voltage and load resistance. A simple shunt regulator is shown in Figure 25 below.

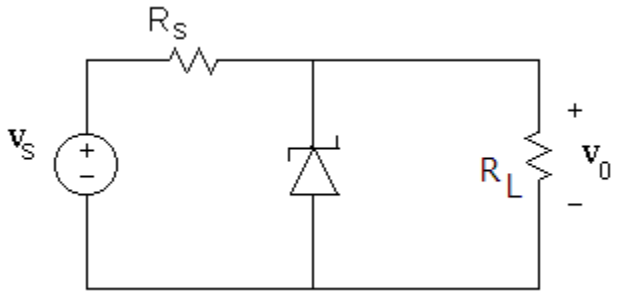


Figure 25: Zener Shunt Voltage Regulator

Let's assume that the components V_S, R_S and R_L are sized such that the zener is in the reverse breakdown region. Using the constant voltage drop model, we replace the zener with a battery as shown in Figure 26.

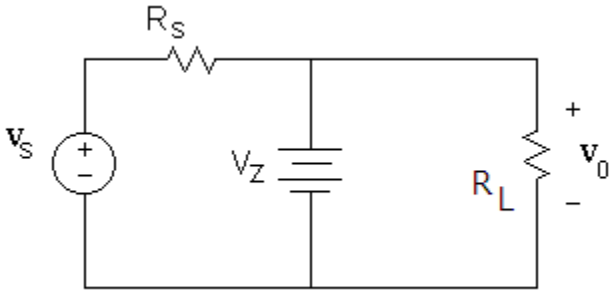


Figure 26: Regulator with Zener Modeled as a Voltage Source

Note that the load resistor is in parallel with the "battery". Assuming that the zener remains in the reverse breakdown region, we can see that the load voltage is not dependent on changes in either R_L or V_S. This is an ideal voltage regulator and is not achievable in practice – remember that we use a battery to model the behavior of the zener which is an idealization. We will introduce a more accurate model shortly.

The ability of the regulator to produce a nearly constant voltage despite changes in the source voltage Vs is called source regulation. The ability to produce a nearly constant voltage despite changes in load resistance is called load regulation. We will examine these parameters after introducing a more accurate model for the zener.

Simulation: Voltage Regulator

Zener diodes - the battery plus resistance model

How can we more accurately model the non-vertical I-V characteristic of the zener in the reverse breakdown region? We see that as the zener diode current increases, the voltage across the zener increases (see Figure 27). Note that the slope in the reverse breakdown region is amplified for illustration.

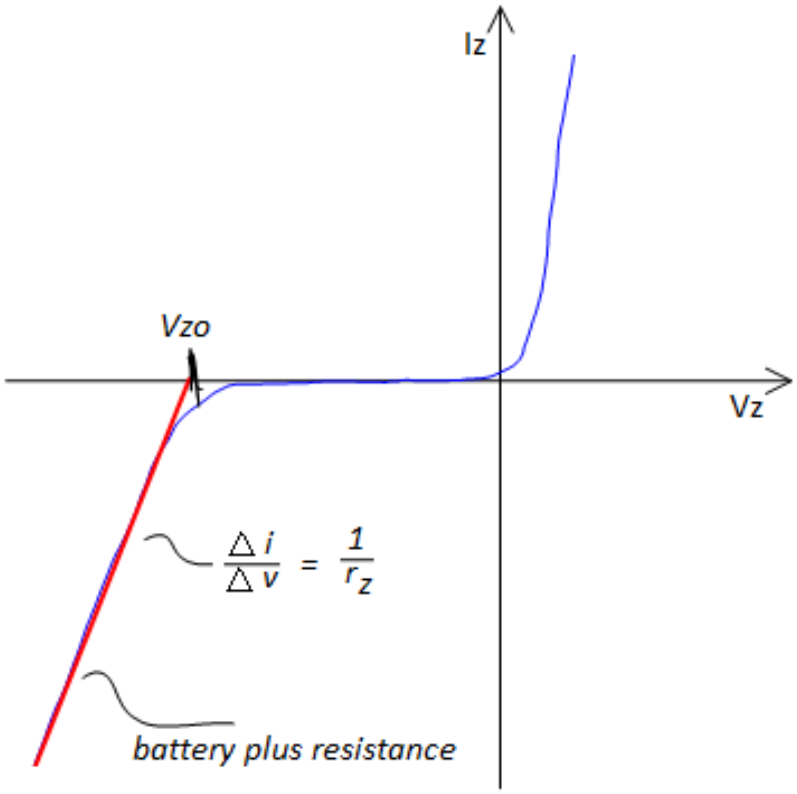


Figure 27: Zener I-V Characteristics Showing Incremental Resistance

In order to model this characteristic we add a small resistance in series with the battery so that as the current increases, the voltage will also increase slightly (see Figure 28). We call this the "battery plus resistance" model and is valid only is in the reverse breakdown region.

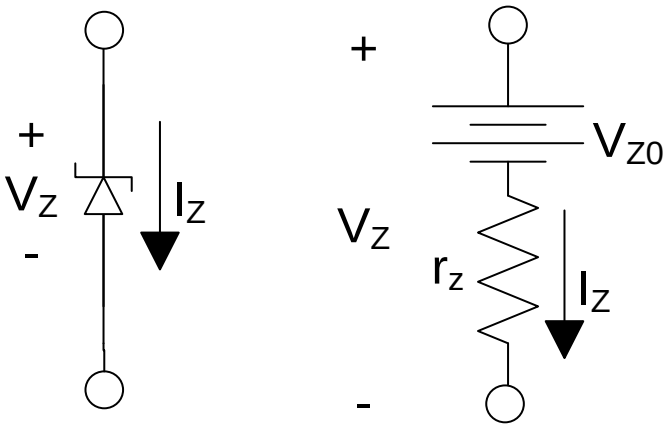


Figure 28: Battery Plus Resistance Model for Zener

The value of r_z is determined from the slope of the I-V characteristic curve and is equal to the inverse of the slope of the line.

$$r_Z = \frac{\Delta v_Z}{\Delta i_Z}$$

Now let's examine the source regulation of a voltage regulator circuit. We will begin with a very simple circuit, one where the load resistance is infinite as shown in Figure 29.

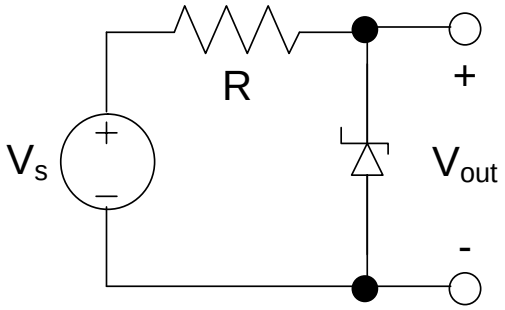


Figure 29: Shunt Regulator with Load of Infinite Resistance

We will start with load line analysis to get a qualitative feel for how changes in source voltage affect output voltage. Then we will use the battery plus resistance model and calculate the source regulation for the voltage regulator.

We construct the load line with the V_S and R_S parameters. We will assume that V_S is not constant but fluctuates slightly by ΔV_S. We plot the load lines at the maximum and minimum V_S (see Figure 30). Notice that the output voltage varies by ΔVo. A zener diode having a more vertical I-V characteristic will result in smaller output voltage changes and therefore better source regulation. It should be noted that slope of the line in the graph below has been exaggerated to more clearly illustrate this concept.

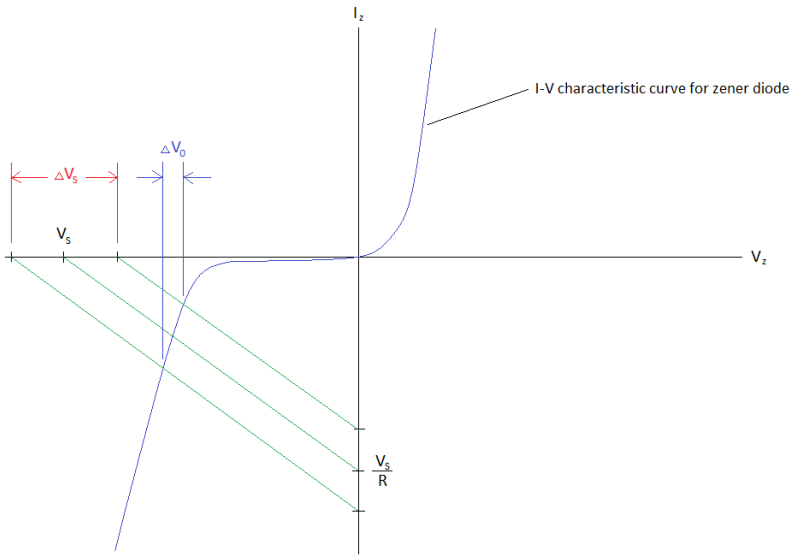


Figure 30: Load Lines for Voltage Regulator

Source Regulation

We now will substitute the battery plus resistance model to calculate the source regulation for the voltage regulator (see Figure 31). Source regulation is a measure of how stable the output voltage is despite changes in source voltage. Ideally, the source regulation would be 0%.

$$Source\ Regulation\ (SR) = \frac{\Delta v_L}{\Delta v_S} \times 100\%$$

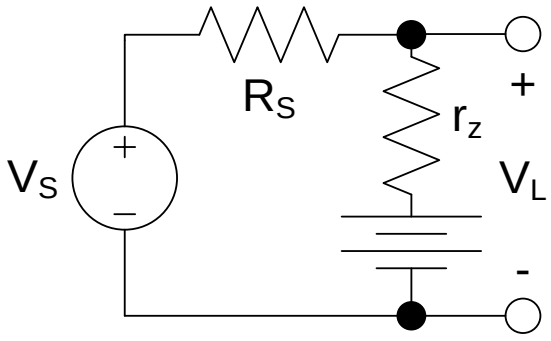


Figure 31: Source Regulation

We can calculate V_L as:

$$V_L = v_z + Ir_z$$
$$V_L = v_z + [(V_S - v_z)/(R_S + r_z)]r_z$$

We find the source regulation by taking the derivative of the output voltage with respect to the source voltage and obtain:

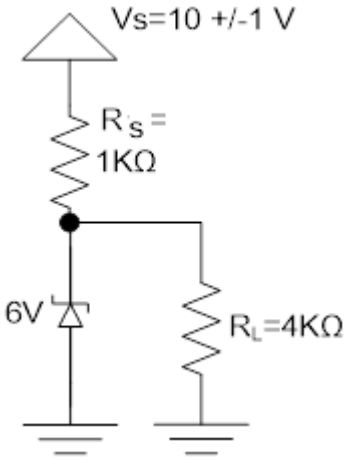
$$\frac{dv_L}{dv_S} = \frac{r_z}{(R_s+r_z)}$$

$$Source\ Regulation = \frac{r_z}{(R_s + r_z)} \times 100\%$$

Note that better source regulation is achieved when $r_z << R_s$.

Example 13: Source Regulation

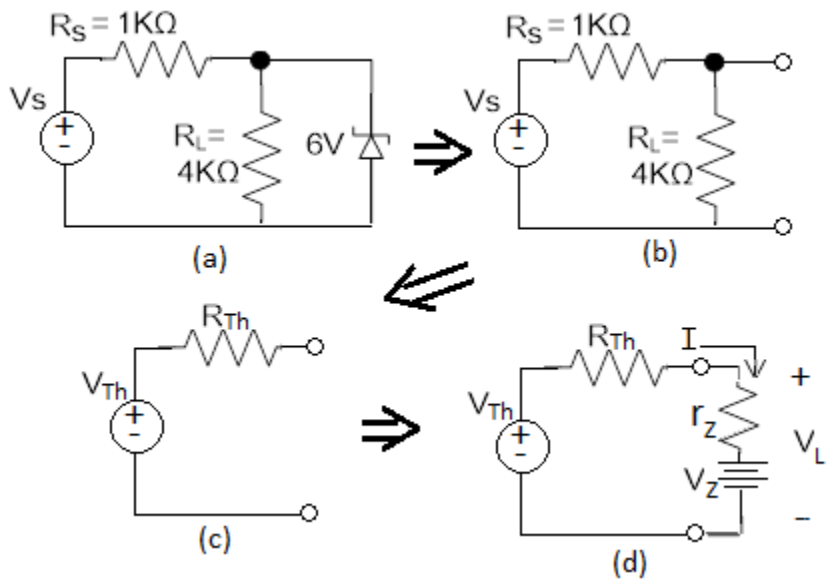
The zener diode in the circuit below has the following specifications: V_Z=6 V, R_L = 4 kΩ and r_z= 20 Ω. The source voltage is nominally 10 V but differs by ±1 V. Find the source regulation for this circuit.



We cannot use the formula derived for the circuit in Figure 31 because that circuit had infinite load resistance. Instead we will determine V_L when Vs is at its maximum and minimum and then divide by the difference in source voltage. Using Thevenin's theorem will help simplify the analysis. It's easier to visualize the Thevenin equivalent that the zener diode sees by swapping the positions of the load resistor and the zener diode. Note that

$$V_{Th} = V_{OC} = Vs\left(\frac{4k}{4k + 1k}\right)$$

$$R_{Th} = R_L // R_S = \left(\frac{4k \times 1k}{4k + 1k}\right) = 800\ ohms$$



From (d) in the figure above, the load voltage with the zener in place can be calculated using:

$$V_L = v_z + Ir_z = v_z + [(V_{Th} - v_z)/(R_{Th} + r_z)]r_z$$

For V_S=11V:

$$V_{Th} = 11\left(\frac{4k}{4k + 1k}\right) = 8.8\ V$$

$$V_{L1} = 6 + 20\left(\frac{8.8 - 6}{20 + 800}\right) = 6.060\ V$$

For V_S=9V:

$$V_{Th} = 9\left(\frac{4k}{4k + 1k}\right) = 7.2\ V$$

$$V_{L2} = 6 + 20\left(\frac{7.2 - 6}{20 + 800}\right) = 6.029\ V$$

$$SR = 100\% \times \left(\frac{\Delta V_o}{\Delta V_s}\right)$$

$$SR = 100\% \times \left(\frac{6.060 - 6.029}{11 - 9}\right)$$

$$SR = 1.54\%$$

Note that the 2 V swing in the source voltage results in only a 0.031 V change in the output voltage.

Load Regulation

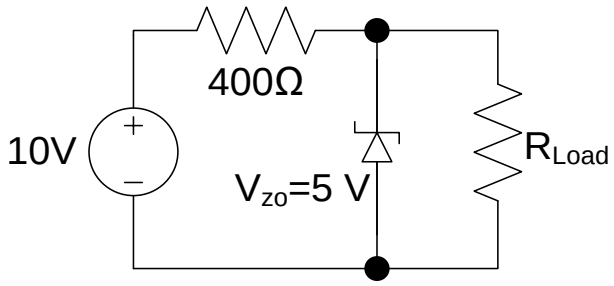
Load regulation is a measure of how much the output voltage changes in response to load current fluctuations and is defined as:

$$Load\ Regulation\ (LR) = \frac{v_{L(no\ load)} - v_{L(full\ load)}}{v_{L(full\ load)}} \times 100\%$$

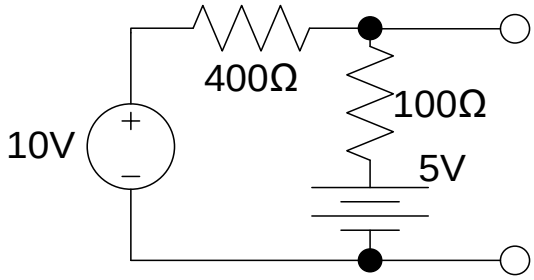
The no load condition is when the load draws no current (infinite resistance) and the full load condition is when the load is at its expected maximum current draw (minimum resistance).

Example 14: Load Regulation

Find the load regulation of the following voltage regulator circuit. Assume V_Z = 5 V and r_z=100 Ω. Assume that the full load current draw is 5 mA.



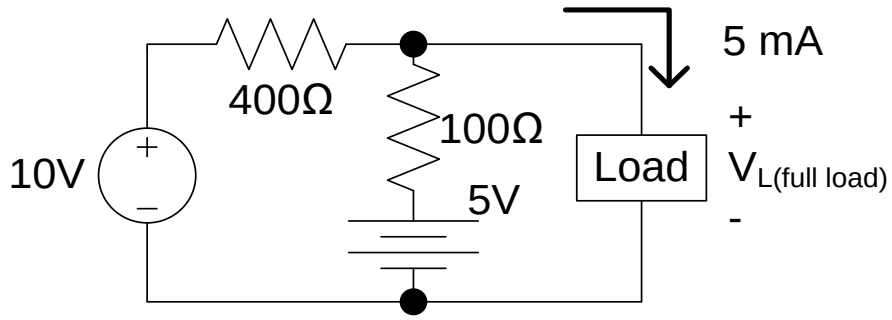
We begin by finding the load voltage when the load is replaced with an open circuit.



$$I = \frac{10 - 5}{400 + 100} = 10\ mA$$

$$V_{L(no\ load)} = 5 + (0.1k)(10m) = 6\ V$$

Next we calculate the full load voltage $V_{L(full\ load)}$ using the circuit below. For full load conditions the load draws 5 mA.



Using KCL at the top node (currents expressed in mA):

$$\frac{v_{Fl} - 10}{0.4} + \frac{v_{Fl} - 5}{0.1} + 5 = 0$$

$\boldsymbol{V_{FL} = 5.6\ V}$

Resulting in a load regulation (LR) of:

$$LR = \frac{6 - 5.6}{5.6} \times 100\%$$

$$LR = 7.14\%$$

This analysis assumed that the zener is in the reverse breakdown region. To verify, we need to make sure the current is biasing the zener in this region. Since the load voltage is higher than the zener voltage we can determine the current is indeed flowing downward through the diode in the reverse bias direction. If it weren't, the regulator would have to be redesigned. How?

By increasing V_S, or decreasing R_S.

Design of a voltage regulator circuit

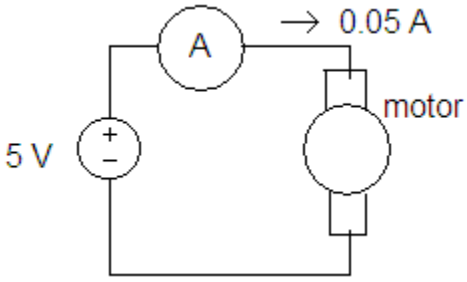
When designing a voltage regulator circuit, we must select R_S and V_S such that the zener is biased in the reverse breakdown region. If V_S is too small, or the load draws too much current (because R_S is too small), the Zener will not operate in the reverse breakdown region and the voltage regulator will not work properly. Another design consideration is that we must select the zener and R_S such that they are capable of dissipating the power that they will absorb. Power dissipation limits can be found on the component data sheet.

Simulation: Effect of R_L on Voltage Regulation

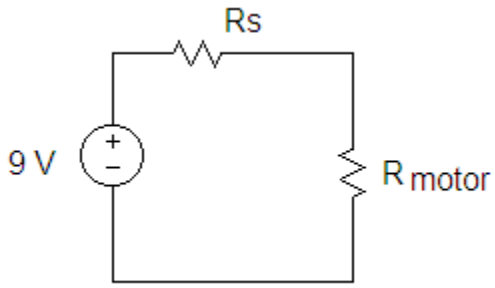
Example 15: Design of a Voltage Regulator

Assume that we have a DC motor that we would like to operate at 5 V DC. We have only a 9 V battery to power this motor so we need to design a circuit that will provide the 5 V that we desire. In order to design the circuit, we begin by determining the motor resistance by using a power supply and an ammeter. We apply a test voltage across the motor terminals of 5 V and we measure the current through the motor and determine it to 0.05 A. From this data we determine:

$$R_{motor} = \left(\frac{5}{0.05}\right) = 100\ \Omega$$



There are 2 designs that we will investigate to supply the 5 V to the motor; a voltage divider circuit and a regulator using a zener diode. We begin with the voltage divider design shown below.



Using voltage division, we can determine the R_S that results in the desired motor voltage.

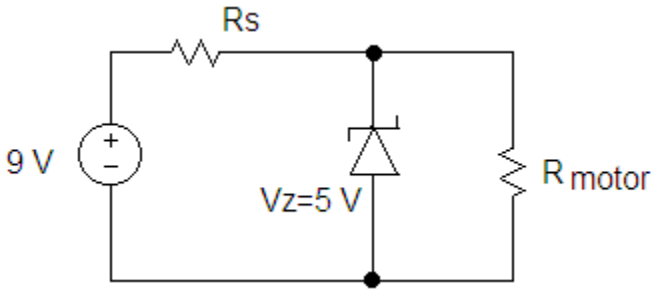
$$V_{motor} = V_{source}\left(\frac{R_{motor}}{R_{motor} + R_s}\right)$$

Solving for R_S yields:

$$R_s = R_{motor}\left(\frac{V_{source}}{V_{motor}}\right) - R_{motor}$$
$$R_s = 100\left(\frac{9}{5}\right) - 100$$
$$R_s = 80\ \Omega$$

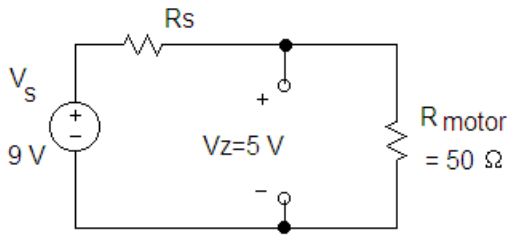
Using a voltmeter, we find that our circuit works quite well until we load the motor (for instance, if we squeeze the shaft of the motor to slow its rotation, we find that the motor voltage drops considerably). The reason for this is that the motor resistance is not constant; it depends upon the output torque of the motor. The more torque the motor provides, the less its resistance and hence it draws more current.

The voltage divider design has poor load regulation compared to the shunt voltage regulator design shown in the circuit below.



This circuit provides a voltage of 5 V to the motor and is less dependent of the motor's resistance. The value of resistor R_S must be selected carefully in order for the circuit to work properly. For instance, if we make R_S too small, the current through the zener diode will exceed its allowable limit. If we select R_S too high, we put the zener in the "off" state instead of reverse breakdown.

We now examine how to determine the upper range limit for R_S. This value is determined by finding the value of R_S such that the zener is placed on the boundary of the reverse breakdown region and the cutoff region. We should calculate R_S from the worst case scenario, when the motor resistance is lowest this will draw more current and tend to place the zener in cutoff. Assume we determine that the smallest R_{motor} we expect is 50 Ω. From this, we can construct the circuit model below. Note that we have set the zener to be on the edge between its off state and reverse breakdown (I_Z=0, V_Z=5 V). Since I_Z=0, we replace the zener with an open circuit.



Because I_Z=0, the two resistors are in series and we can use voltage division to determine the value of R_S.

$$V_{motor} = V_s\left(\frac{R_{motor}}{R_{motor} + R_s}\right)$$

Solving for R_s yields:

$$R_s = R_{motor}\left(\frac{V_s}{V_{motor}}\right) - R_{motor}$$
$$R_s = 50\left(\frac{9}{5}\right) - 50$$
$$R_s = 40\ \Omega$$

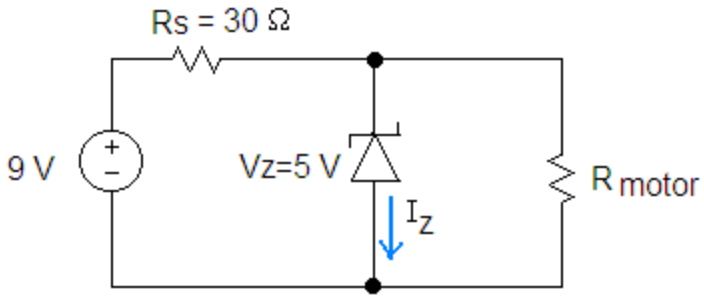
Therefore, the value of R_S must be a maximum of 40 Ω because exceeding this value would put the zener in the "off" state when the motor draws its maximum current. A value less than 40 Ω will place the zener in the desired reverse breakdown region. Since we want to ensure that the zener is in the reverse breakdown region, we might choose a value such as 30 Ω to provide a safety margin to allow for resistor tolerance and temperature effects. To determine the required power rating of the resistor we perform the following calculations:

$$I = \frac{9 - 5}{30} = 0.133\ A$$

$$P = I^2R$$
$$= (0.133)^2 \times 30$$
$$= 0.533\ W$$

Therefore, we should select a 30 Ω resistor with a power rating of 1 W. Of course we could choose R_S less than 30 Ω but this would have the effect of sending more current through the zener which will require it to dissipate more power.

Let's now calculate how much power the zener must dissipate with this design.



What value of R_{motor} should we choose in order to perform this calculation?

> ***We should choose the "worst case" value - the one that would result in higher zener current. In this case - it is the highest R_{motor}, which would be the motor resistance of 100 Ω because a larger R_{motor} results in more current through the zener and hence greater power dissipation.***

To determine the zener current we use KCL:

$$I_Z + I_S + I_{motor} = 0$$

$$I_Z + \frac{(5-9)}{30} + \frac{5}{100} = 0$$

$$I_Z = 83.3\,mA$$

Next we calculate the power dissipated in the zener.

$$P_{zener} = I \times V$$

$$P_{zener} = (0.083)(5) = 0.4165\,W$$

This is the maximum power dissipation required of the zener – the power that must be dissipated when the motor resistance is at its highest. We should select a zener that is capable of dissipating at least 0.5 W. Selecting a 1 W zener would be safer.

Small Signal Model

Electronic circuits are often used for processing signals that are time varying (AC). Typically, they need to be biased with DC in order for them to process the AC signal. For instance, in later chapters, we will see that transistors can be used to amplify signals but the transistors must be biased with DC in order to perform the amplification. To analyze such circuits, we will find it convenient to separate the analysis into DC and small signals. We perform the DC analysis to ascertain how the electronic circuit is biased (it's DC operating point) and then once this is done, we perform a small signal analysis to determine the ac output signal.

Although small signal analysis of diodes is of limited usefulness, we will find the technique very useful with transistors. Because diodes are much simpler, this is a good time to introduce the concept of small signal analysis.

To understand small signal analysis, let's perform a conceptual experiment. We will attach a voltage source across a diode that is composed of a DC component and a small signal (AC) component (see Figure 32). Small signal analysis will allow us to determine the small signal current (i_d) that is caused by the small signal voltage (v_d). We use the following notation:

v_D is the total voltage, V_D is the DC voltage, and v_d is the small signal voltage. The same use of lower and upper case letters is used for currents.

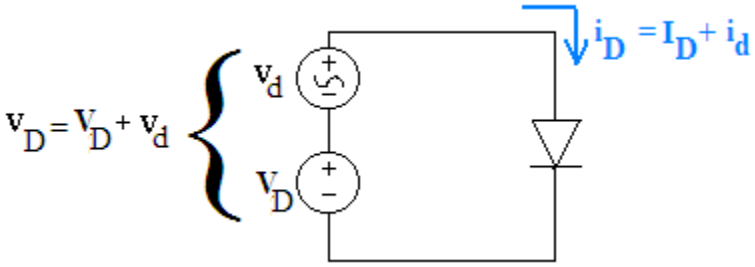


Figure 32: Small Signal Analysis

The idea behind small signal analysis is that the analysis can be separated into parts; first we find the DC operating point, then we use small signal analysis to determine the small signal current resulting from the small signal voltage.

The graph below (Figure 33) is used to illustrate this idea more clearly. The DC operating point is given by (V_D, I_D). Note that the ac voltage source causes v_D to fluctuate by Δv. This fluctuating voltage causes the current to fluctuate by Δi. The small signal voltage causes the operating point to move along the diode characteristic curve. For small changes in voltage, we can approximate the curve as a straight line given by the slope of the curve at the DC operating point. The inverse of this slope is called the incremental resistance r_d and is used to model how the diode current changes in response to changes in diode voltage. Next we examine how to determine the incremental resistance and how we use small signal analysis to analyze diode signal response.

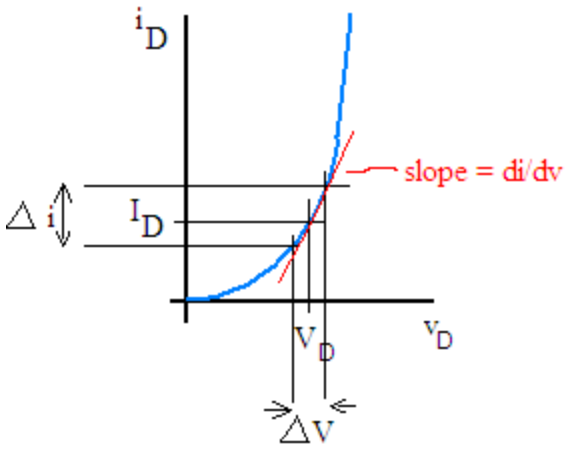


Figure 33: Small Signal Analysis - Slope at Q Point

The slope of the curve at the DC operating point or Q-point is:

$$slope = \left.\frac{di_D}{dv_D}\right|_{Q\ point}$$

For small changes in Δv_D we can write:

$$slope = \left.\frac{di_D}{dv_D}\right|_{Q\ point} \cong \frac{\Delta i_D}{\Delta v_D}$$

We define the incremental resistance r_d as

$$r_d = \left\{\left.\frac{di_D}{dv_D}\right|_Q\right\}^{-1}$$

Therefore we can write:

$$\Delta v_D = r_d \Delta i_D$$

Since Δv_D and Δi_D represent the small signal voltage and small signal current, we can write:

$$v_d = r_d i_d$$

Therefore, for small signals, the diode acts like a resistor. That is, as the current increases, the voltage does as well. The greater the slope of the line at the operating point, the smaller the incremental resistance.

To find the incremental resistance, we use the Shockley equation to determine the slope of the curve. The diode I-V characteristic curve can be approximated using the simplified Shockley Equation:

$$i_D = I_S\ (e^{v_D/V_T})$$

Now we find the slope of the curve at the DC operating point or Q-point.

$$\left.\frac{di_D}{dv_D}\right|_Q = \left[\frac{1}{V_T}\left(I_S\ (e^{v_D/V_T})\right)\right]_Q$$

Evaluating this expression at the Q-point (where $v_D=V_{DQ}$) we can write:

$$\left.\frac{di_D}{dv_D}\right|_Q = \left[\frac{1}{V_T}\left(I_S\ (e^{V_{DQ}/V_T})\right)\right]$$

Note that:

$$I_{DQ} = I_S\ (e^{V_{DQ}/V_T})$$

Therefore:

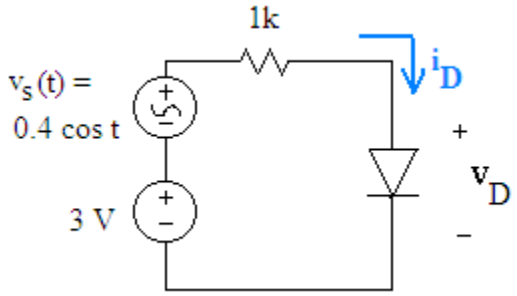
$$\left.\frac{di_D}{dv_D}\right|_Q = \frac{I_{DQ}}{V_T}$$

Since r_d is the inverse of the slope of the line at the Q-point:

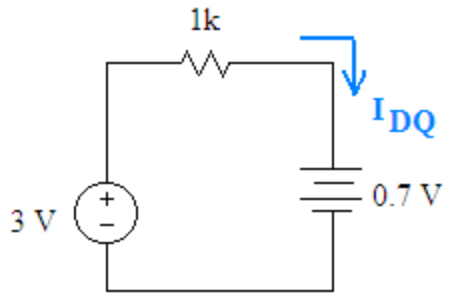
$$r_d = \frac{V_T}{I_{DQ}}$$

Example 16: Small Signal Analysis – Finding the Incremental Resistance

Find the incremental resistance r_d of the diode in the circuit below. Assume $Is=10^{-14}$ A and $V_T=25$ mV:



To find resistance r_d we must find the dc operating current I_{DQ}. This value if found by ignoring the small signal component and finding the current I_D caused by the DC voltage source. There are many models that we can choose from to find the current I_D (ideal model, constant voltage drop model, and exponential model). A nice balance between ease of use and accuracy is the constant voltage drop model. The result is the DC model of the circuit shown below:



By inspection, we see that I_{DQ} = 2.3 mA.

We can now calculate r_d:

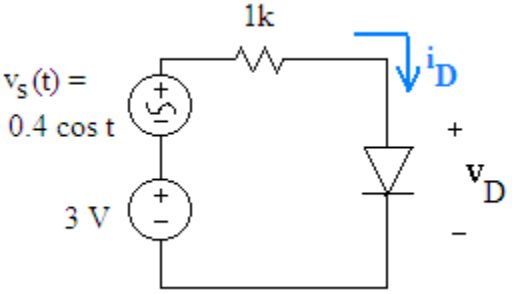
$$r_d = \frac{V_T}{I_{DQ}}$$

$$r_d = \frac{25m}{2.3m}$$

$$r_d = 10.9\ \Omega$$

Example 17: Small Signal Analysis - Finding Small Signal Output

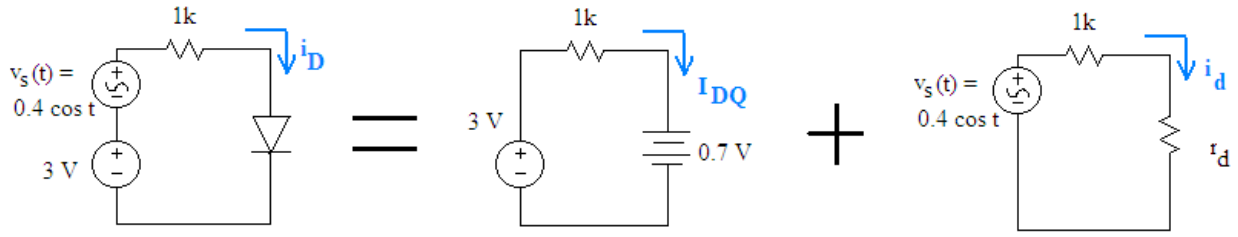
Find the current i_D using small signal analysis.



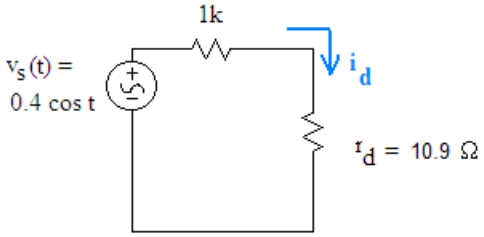
We are asked to find the i_D which is composed of both DC and AC components.

$$i_D = I_{DQ} + i_d$$

The figure below illustrates how we separate the analysis into DC and small signal models.



We start with the DC analysis and find I_{DQ}=2.3 mA as we did in the previous example. Using the incremental resistance equation we find r_d=10.8 Ω. Next we create the small signal model of the circuit by replacing the resistor with its incremental resistance r_d.



To find i_d we use Ohm's law:

$$i_d = \frac{v_s(t)}{R + r_d}$$

$$i_d = \frac{0.4 \cos t}{1000 + 10.9}$$

$$i_d = \{0.396\ cos\ t\}\ mA$$

And now we determine the total current i_D:

$$i_D = I_{DQ} + i_d$$

$$i_D = \{2.3 + 0.396\ cos\ t\}\ mA$$

The simulations below illustrates the small signal model concept.

Simulation: Small Signal Model

Simulation: Small Signal Model #2

We conclude the chapter with a look at a diode application that combines a diode rectifier with a zener based shunt regulator.

AC to DC Conversion

We now examine a very common and important diode application – AC to DC voltage conversion. The device that charges your cell phone (and many other appliances) must include circuitry that converts AC voltage to DC voltage. The process of converting AC to DC is depicted in the Figure 34 below. The graphs depict the voltage at each state of the conversion process. We will describe each stage briefly.

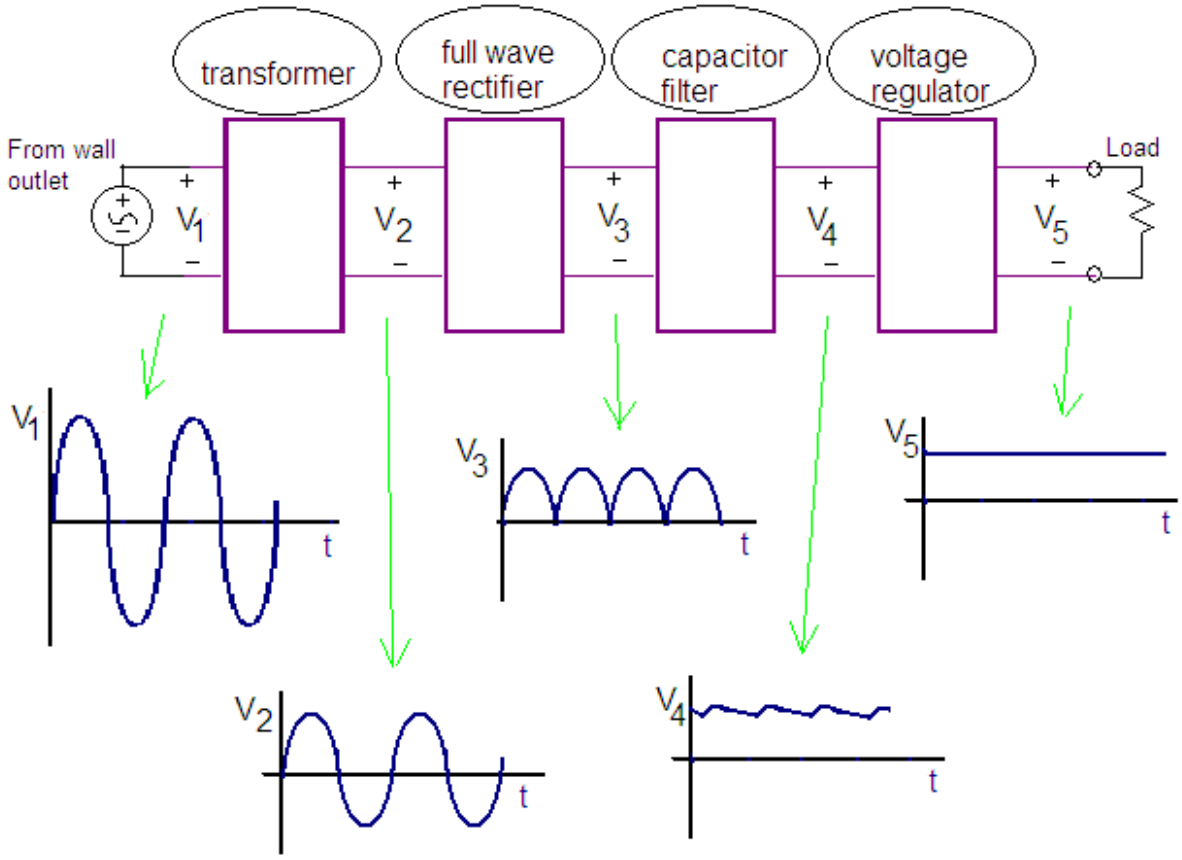


Figure 34: AC to DC Conversion

The first stage of the conversion process uses a transformer - a device that takes an input AC waveform (V_1) and changes its magnitude (V_2). For typical wall transformers, the goal is to step down the voltage. For instance, the transformer could take the 170 V magnitude AC waveform from the wall outlet and step it down to 17 V. (A sine wave of 170 V is approximately equal to 120 V_{RMS} the measurement that you may be familiar with). The transformer steps up or down the voltage using magnetic coupling. A primitive transformer is shown in Figure 35 below.

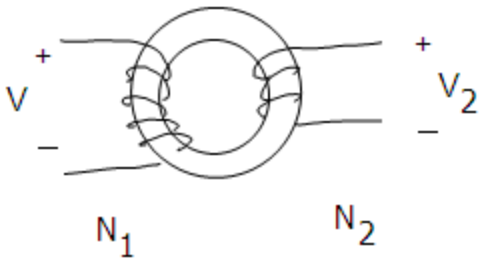


Figure 35: Primitive Transformer

Transformers use different number of turns of wire on the two sides to step up or down the voltage to the desired level. The relationship between voltage (V) and turns of wire (N) is given by the ideal transformer equation:

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

Note that there are fewer coils of wire (turns) on side 2 than side 1 of the transformer shown in Figure 35, consequently the output voltage V_2 will be less than the input V_1. (Ideally the transformer loses no power, so if the voltage is stepped down, the current is stepped up). If you have not already studied transformers, you will learn more about them in a future course.

Simulation: Step Down Transformer

The second component shown in the AC to DC converter is the full wave rectifier which was described in an earlier section.

The third stage is the capacitor filter which keeps the voltage steadier. You can think of charge in a capacitor like water in a lake - charge may be added or subtracted from the capacitor but its voltage changes slowly just like the water level of a lake will change slowly as water flows into or out of the lake.

Simulation: Capacitor Charge and Discharge Rates

As the voltage from the bridge rectifier is greater than the capacitor voltage, the capacitor will charge very quickly and approximate the input voltage until it reaches its peak. As the input voltage drops, the capacitor will slowly discharge. The rate of discharge is dependent upon the value of the capacitor (its capacitance) and the resistance of the circuit to the right. The smaller the resistance, the greater the discharge current and the more quickly the voltage of the capacitor will drop. Using the lake analogy, the larger the lake, the more slowly its level will decrease. The larger the stream that is flowing out of the lake (analogous to low resistance) the faster the lake level (analogous to voltage) decreases.

The final stage in the AC to DC converter is the voltage regulator that produces a nearly constant DC voltage. The input voltage coming from the capacitor stage fluctuates a little bit, but the

output of the rectifier maintains an almost constant output voltage because of its source regulation and load regulation properties.

Simulation: AC to DC Converter

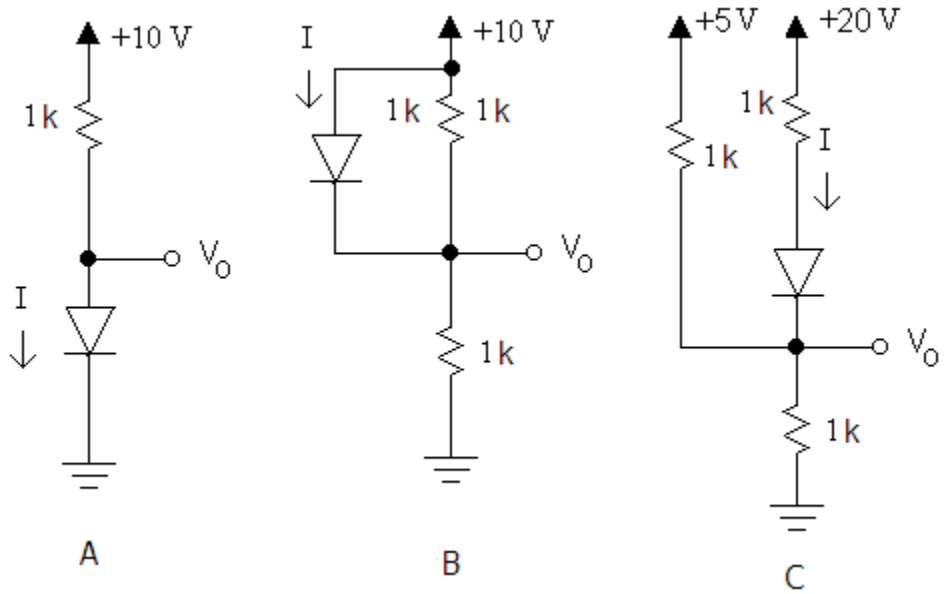
Simulation: AC to DC Converter with Transformer

Summary

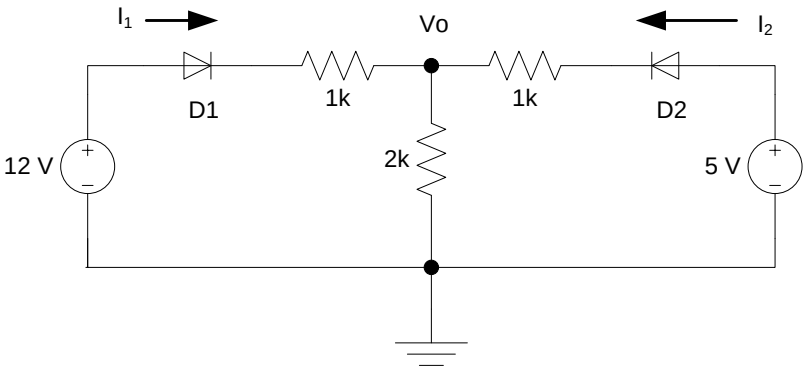
1. Diodes are very useful devices found in nearly all electronic devices.
2. Diodes pass current freely in one direction but block current from flowing in the opposite direction.
3. There are several models that can be used to describe the behavior of the diode: ideal model, constant voltage model, exponential model (Shockley equation).
4. When analyzing DC diode circuits, we must make an assumption regarding the state of the diode, calculate circuit values, and then verify our assumption was correct.
5. Load line analysis is helpful for gaining qualitative insights regarding diode biasing.
6. Half wave rectifiers pass the positive half cycles but block the negative portion.
7. Full wave rectifiers pass the positive half cycles and invert the negative portion.
8. Capacitors can be used in conjunction with rectifiers to produce a nearly DC waveform with a slight ripple. The peak to peak ripple depends upon the capacitance and the resistance of the load.
9. LEDs behave similarly to junction diodes but have a greater forward voltage drop.
10. Zener diodes are designed to operate in the reverse breakdown region.
11. Clipper circuits clip off the top and or bottom of an input waveform.
12. Zener diodes can be used in voltage regulator circuits. Two important parameters of voltage regulators are their source regulation and load regulation.
13. Small signal analysis involves separating the DC analysis from the signal analysis. The small signal model of a diode is an incremental resistance.

Problems

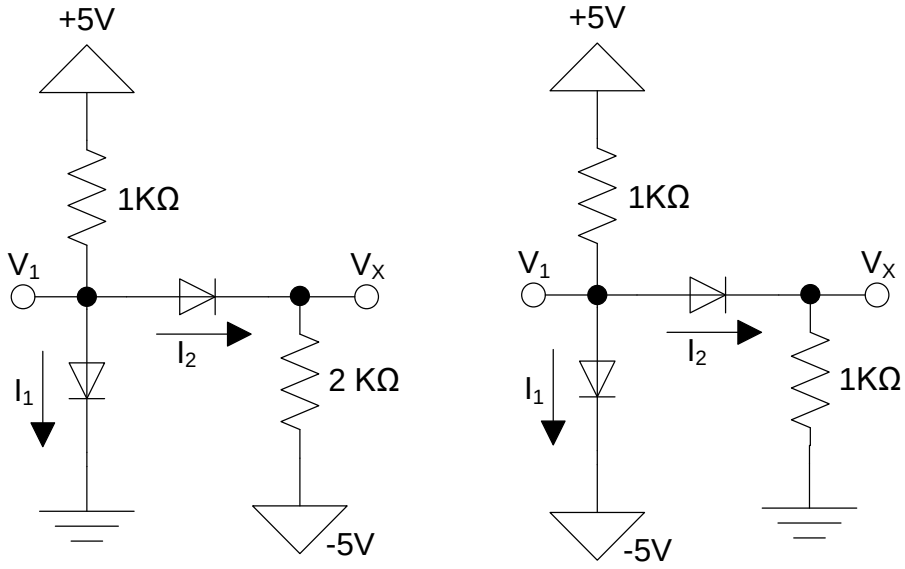
1) Determine the labeled voltages and currents in the circuits below using the ideal diode model. Verify assumptions made regarding diode state.



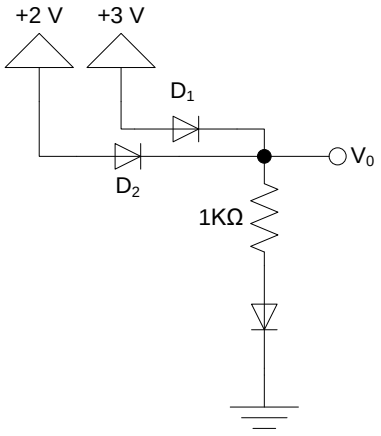
2) Determine the labeled currents and voltages in the circuits below using the ideal diode model. Clearly verify assumptions regarding diode states.

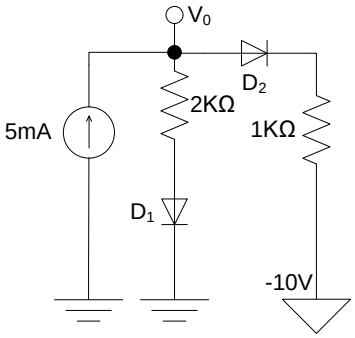


3) Determine the labeled currents and voltages in the circuits below using the ideal diode model. Clearly verify assumptions regarding diode states.

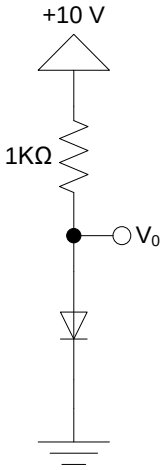


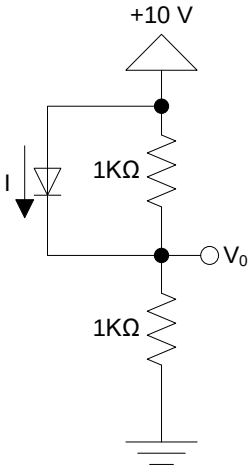
4) Determine the labeled currents and voltages in the circuits below using the ideal diode model. Clearly verify assumptions regarding diode states.

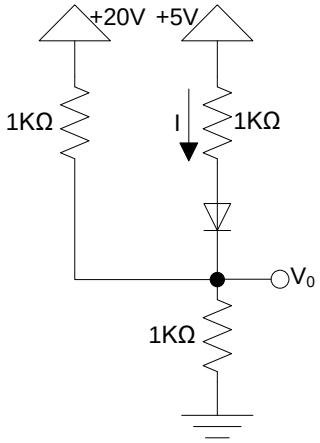




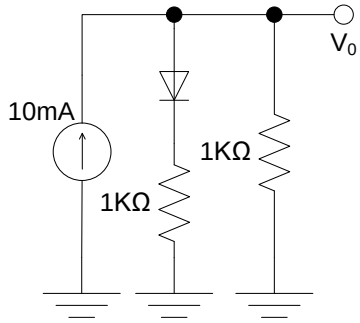
5) Determine the voltage Vo using the constant voltage drop model.

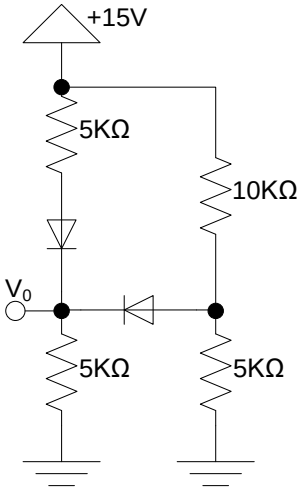


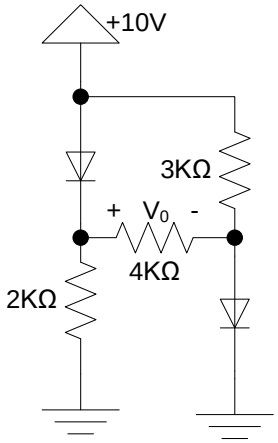




6) For the circuits below, determine the voltage V_O using the constant voltage drop model.



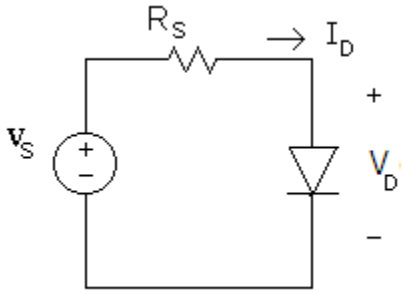




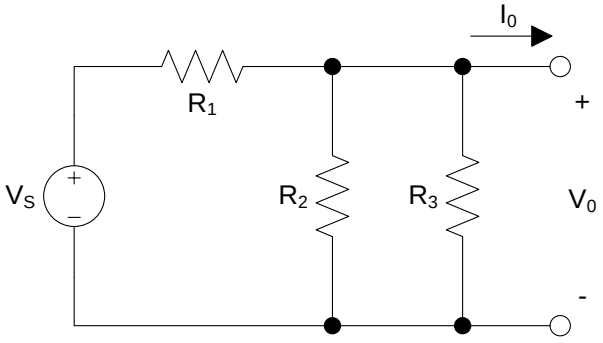
7) A student wishes to power 2 LEDs (one red, one green) with a single microcontroller output pin that can be set to either 0 V or 5 V. When the microcontroller output pin is set to high (5 V) the student wishes to turn on both of these LEDs. The microcontroller is capable of

sourcing 50 mA of current from one of its output pins. The LED currents should be kept below 30 mA (assume 20 mA is a safe current that produces bright illumination). The Red LED has a turn on voltage of 2.2 V and the green LED has a turn on voltage of 2 V. Design a circuit to turn on the LEDs. Draw a clear schematic and clearly specify all component values on the schematic.

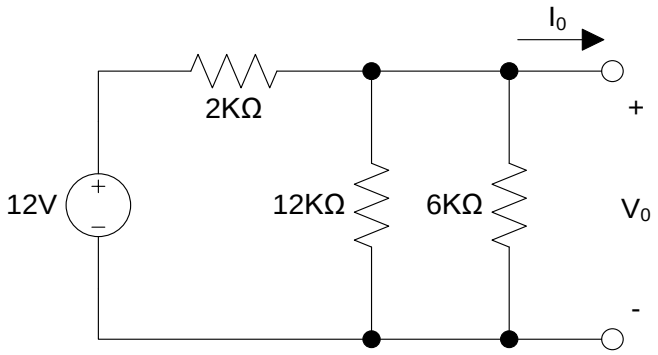
8) For the circuit attached to the diode, draw the load lines for each of the given values on a single graph.
   a) For V_S=10 V and R_S = 1 kΩ
   b) For V_S=10 V and R_S= 2 kΩ
   c) For V_S=5 V and R_S = 1 kΩ
   d) For V_S=5 V and R_S=0.5 kΩ
   e) On the graph, add a characteristic curve for a typical junction diode similar to what has been shown in the text.
   f) Comment on how you could adjust V_S and R_S in order to decrease the current through the diode.



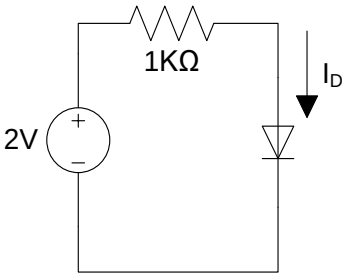
9) Draw a load line for the circuit below. Label the points where the line crosses the horizontal and vertical axes in terms of V_S, R_1, R_2, and R_3. Hint: Use Thevenin's theorem to simplify the circuit.



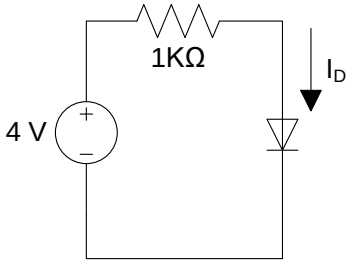
10) Draw the load line for the circuit below. Hint: Use Thevenin's theorem to simplify the circuit.



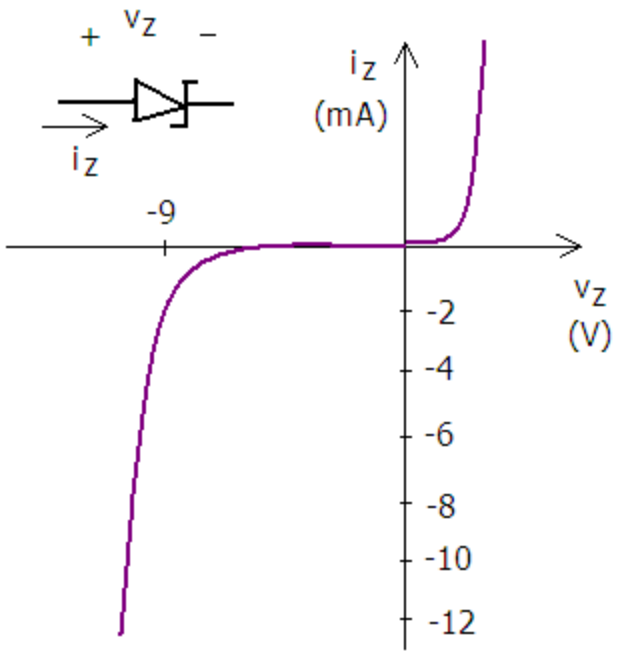
11) A junction diode with $I_S=10^{-14}$ A and $V_T=25$ mV is placed across the source as shown below. Determine I_D using the Shockley equation.

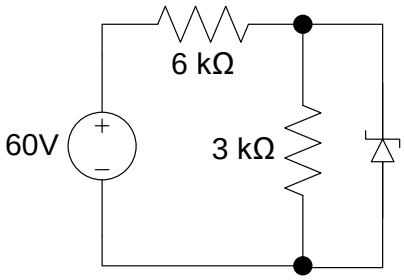


12) Solve for the current in the circuit below using:
   a) The Shockley equation. Assume $I_S=10^{-14}$ A and $V_T=25$ mV.
   b) The constant voltage drop model.
   c) The ideal diode model.
   d) Comment on these analysis techniques in terms of time spent analyzing the circuit and the accuracy of the final answer.

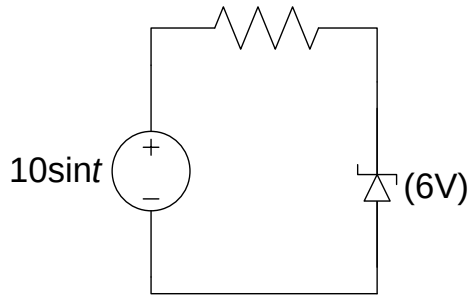


13) A zener diode has an I-V characteristic as given in the graph below. This diode is placed in the circuit shown. Using load line analysis, determine the current through the diode.

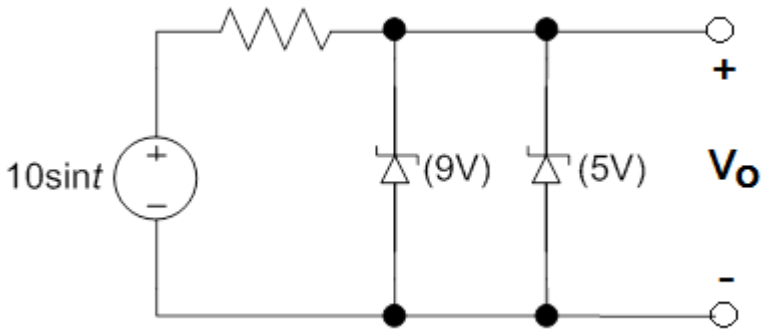




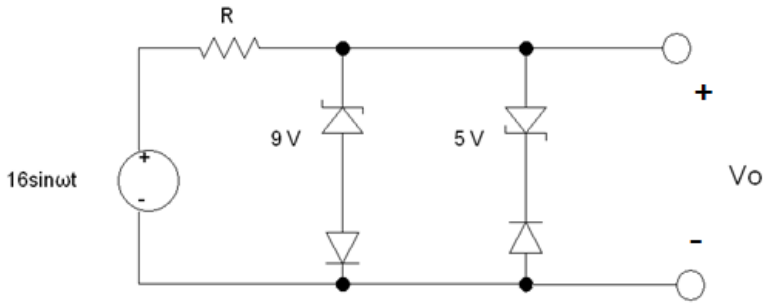
14) Draw the output voltage waveform for the clipper circuit below.



15) Draw the output voltage waveform for the clipper circuit below.

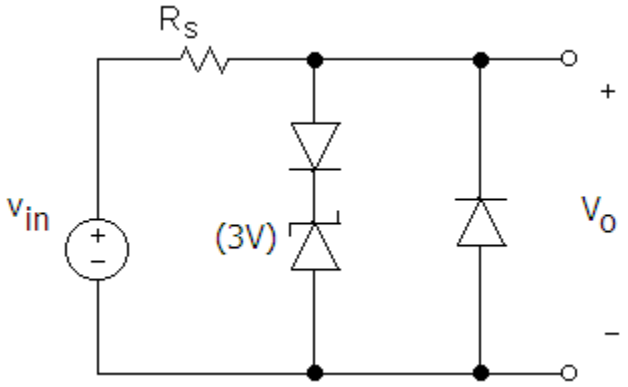


16) Draw the output voltage waveform for the following circuit. Assume the constant voltage drop model for the junction diodes.

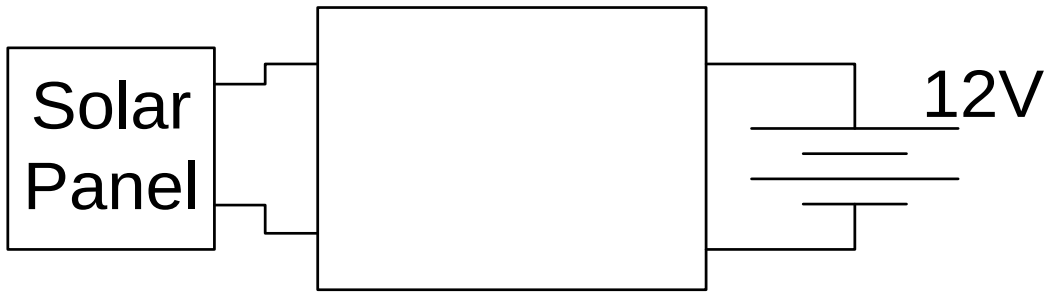


17) Design a clipper circuit that clips off portions of the input waveform that are above 3 V and below -5V. The input voltage is vs=10sinωt V.

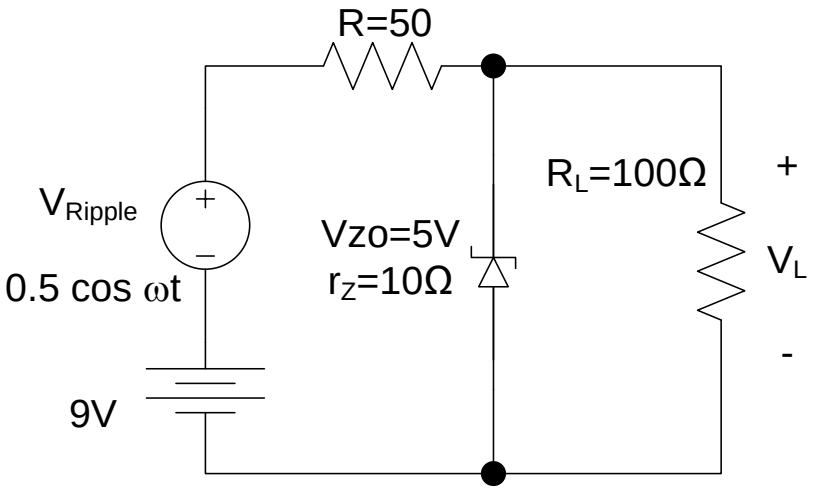
18) Draw the transfer characteristics (v_{out} vs v_{in}) for the circuit below for -5 V < V_{in} < +5 V
   a) Assume the ideal diode model for the junction diodes.
   b) Assume the constant voltage drop model for the junction diodes.



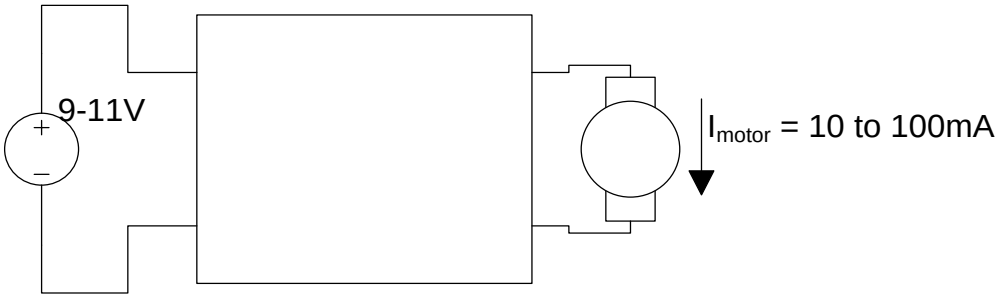
19) The solar panel is to be used to charge the 12V battery. The solar panel will produce a voltage between 18 V at full sun to 0 V at dark. Design a circuit that can be used to charge the 12 battery using a junction diode, a zener diode, and resistor(s).



20) Determine the source regulation of the circuit below. Assume that the zener diode has a dynamic resistance of r_Z = 10 Ω.

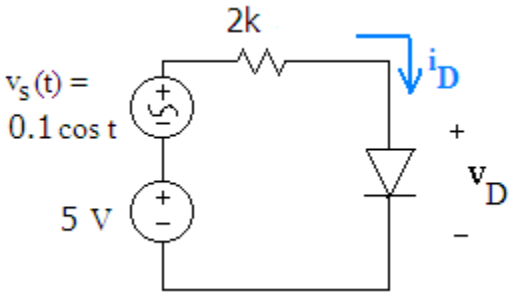


21) Design a voltage regulator circuit that will provide a constant voltage of 5 V to a load from a voltage that is 10 V ±1 V (varies between 9 V and 11 V). The load is a motor whose current varies from 10 mA to 100 mA depending on its torque. Assume ideal zener diodes are available (r_z=0). Draw a clear schematic diagram of the regulator with all element values clearly specified.

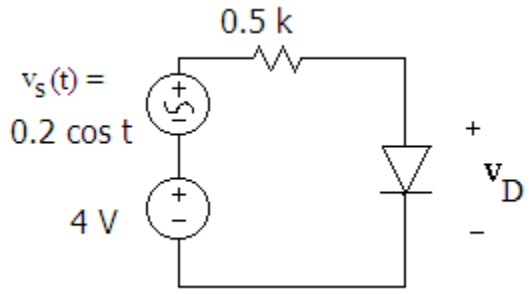


22) Draw the schematic diagram of an AC to DC converter circuit that takes 170V AC and converts it to approximately 12 V DC.

23) Determine the total current through the diode i_D using small signal analysis. Your answer should have a DC term and an AC term!

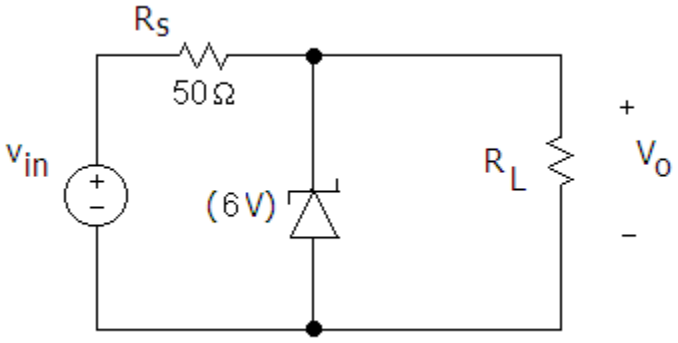


24) Determine the small signal voltage [$v_d(t)$] in the circuit below.



25) Design a small "task light" using LEDs. The light will use a wall outlet for its power source. The LEDs are 100 mA LEDs that have a forward voltage drop of 2 V. Zener diodes are available in a variety of voltage drops, and standard resistor values are available. Optional: Design your light so that it has light setting of dim, medium, bright.

26) Determine the source regulation and the load regulation of the following voltage regulator. Assume r_z=10 Ω. Assume the full load current draw is 100 mA. Assume that V_{in} is nominally 12 V but varies by ± 1 V. When calculating source regulation, assume the circuit is operating with the load at the full-load current draw.



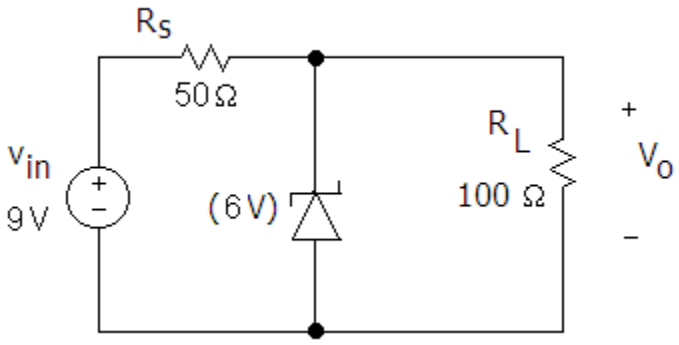
27) Design a 5 V zener voltage regulator that operates from a voltage source that varies from 8 to10 V. The load current varies from 0 to 20 mA.
   a) Determine the value of resistance Rs so that the minimum magnitude of the zener diode current is 5 mA.
   b) What is the maximum value of the zener current?
   c) Assume power ratings for R_S can be ¼ W, ½ W, and 1 W. What is the minimum allowable power rating for R_S?

28) You are stranded on a deserted island with your cell phone which has a dead battery. You have access to bananas (can be used as a resistor), wire, a 9V battery, and lots of junction diodes. Design a voltage regulator to charge your cell phone but not overcharge it. The cell phone battery is a 3.7 V lithium ion battery. The battery charging current should be a maximum of 20 mA. Assume that the minimum battery voltage is currently about 2.5 V. You will be able to use the phone if the battery voltage is above 3.2 V. Design the circuit to

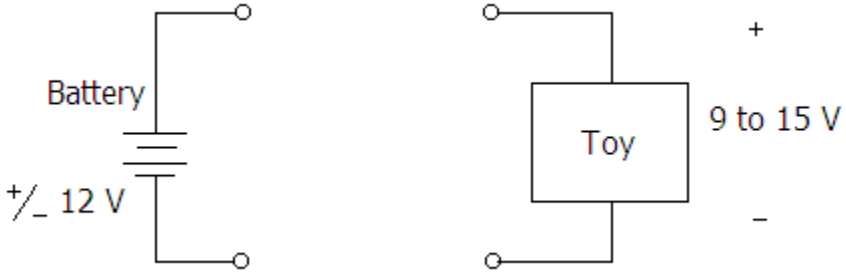
charge your cell phone battery to at least 3.2 V. What would you do once the battery is charged?

29) For the voltage regulator circuit below, Determine the power delivered by the source and the power delivered to the load. What is the efficiency of the circuit?

$$Efficiency = 100\% \times \left({}^{P_{out}}/_{P_{in}}\right)$$



30) A toy is powered with a 12 V battery pack. The toy can operate safely with any voltage from 9-15 V DC. Design a circuit that will prevent the battery from damaging the toy in case a voltage of -12 V is mistakenly applied to the toy.



31) Add a "wrong polarity" LED indicator to the circuit above that will light if -12 V is applied to the toy.

List of Examples

List of Figures

Chapter 3: Field Effect Transistors

Introduction

Transistors are extremely important devices which are found in consumer products such as cell phones, audio components, televisions, computers, GPS units, etc. There are two basic functions that transistors perform – amplification and logic switching. Logic switching is critically important as it forms the basis of all digital circuitry. Before the development of transistors in the 1950s, vacuum tubes were used, but transistors are far superior in terms of reliability, energy efficiency, speed, and cost. While vacuum tubes are still used in some high-end audio applications, transistors have replaced vacuum tubes in nearly every other electronic device.

There are two main types of transistors, the Field Effect Transistor (FET) and the Bipolar Junction Transistor (BJT). BJTs were invented first but FETs have replaced BJTs in many applications because of advantages such as energy efficiency and size.

The most common type of FET is the Metal Oxide Semiconductor Field Effect Transistor or more simply MOSFET. MOSFETs are used in logic circuits, amplifiers, and electromechanical systems such as motor speed control circuits used in robotics and many other applications. In this chapter we will discuss the use of MOSFETs in logic circuits, amplifiers, and motor control.

The MOSFET is a voltage controlled current device where the voltage between two terminals controls the current flow in the third terminal. There are two types of MOSFETs, the n-channel MOSFET and the p-channel MOSFET. We will focus primarily on the n-channel MOSFET or NMOS although the same fundamental concepts apply to both types. The circuit symbol for n and p channel MOSFETS are shown in Figure 36.

MOS transistors can be discreet (see Figure 37) or there can be literally millions of them on a single integrated circuit like the RAM chip shown in Figure 38.

Schematic Symbols for MOSFET	Discreet MOSFET	MOSFET IC (RAM)

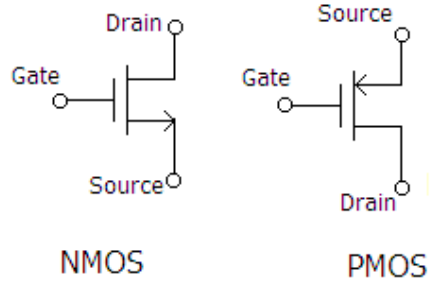



Figure 36: Schematic Symbols for MOSFETs	**Figure 37: Discreet Power MOSFET**	**Figure 38: RAM Integrated Circuit**

Physical Construction of NMOS Transistor

A simplified version of the physical structure of an n-channel enhancement-mode MOSFET (also known as NMOS transistor) is shown in Figure 39: Physical Representation of a MOSFET. The three terminals are the gate (G), the drain (D) and the Source (S). The areas in black are the electrodes where the terminals are connected to the transistor. The dashed area under the gate is a thin layer of insulating material. Because of this insulating material, there is no path for current to flow into or out of the gate. The gate is the control terminal that determines how much current will flow from drain to source.

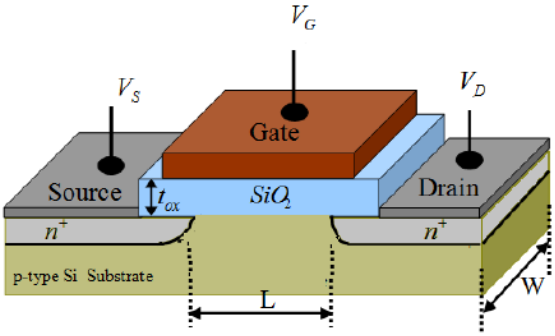


Figure 39: Physical Representation of a MOSFET

We "turn on" the transistor by applying a voltage at the gate. When sufficient voltage is applied, a channel forms under the gate that allows current to flow from the drain to the source (see Figure 40). Once a channel is formed, current will flow provided there is a voltage applied from the drain to source. (It may sound odd for current to be flowing *into* the source rather than *from* it but we define current as the movement of positive charge. The negatively charged electrons actually do flow from source to drain.)

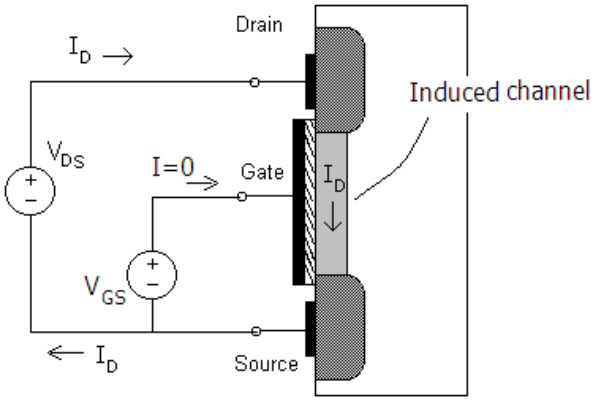


Figure 40: MOSFET with Induced Channel

The amount of current flowing from drain to source is dependent upon the voltages V_{GS} and V_{DS} where V_{GS} turns on or off the transistor and V_{DS} provides the push to move current from drain to source. The current also depends upon the physical properties of the transistor which we discuss briefly in the next section.

Transistor Parameters

We will see shortly that the equations governing current flow from drain to source contain a term called the "transconductance parameter" K_n which depends on the physical properties of the transistor.

$$K_n = \frac{1}{2} k' \frac{W}{L}$$

Note that K_n contains three variables; k' which depends on the fabrication technology - over which the engineer has limited control - and the geometric properties width (W) and length (L) of the channel. These geometric properties can be specified by the engineer to produce desired properties. For integrated circuits, L and W can be different for different transistors on the same silicon chip while k' will remain constant over the entire chip.

Modes of Operation

The transistor has three distinct modes of operation that depend on the voltages applied to the terminals. Recall that in an ideal diode there are two modes of operation, forward bias and reverse bias. In a MOS transistor, there are three modes of operation for the transistor; cutoff, triode, and saturation. We will illustrate these modes in the sections below with a conceptual experiment. In the experiment, we apply variable voltages from gate to source and from drain to source as shown in Figure 41 below and note the resulting drain current (I_D).

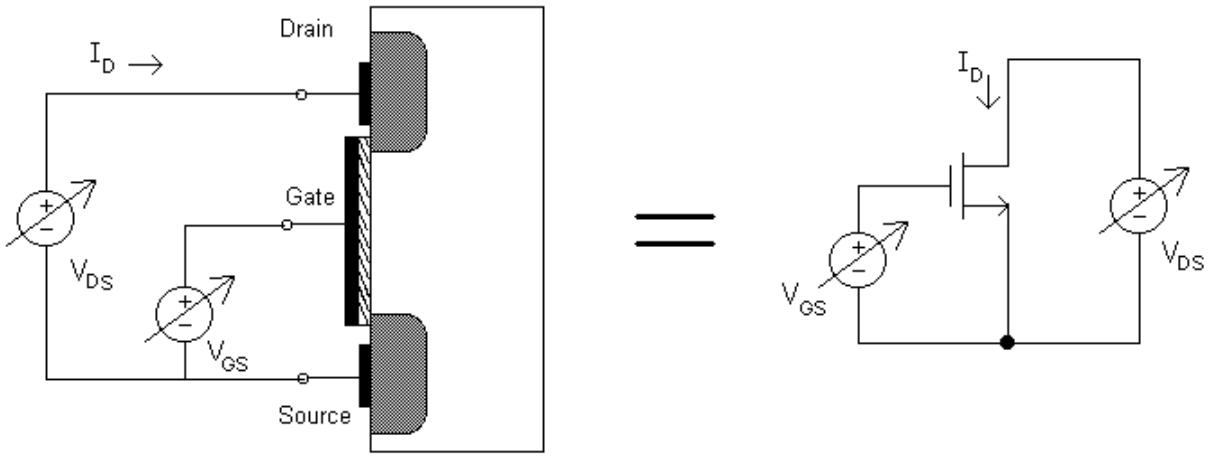


Figure 41: Setup to Investigate MOSFET Modes

Simulation: First Look at a MOSFET

Cutoff

We begin the experiment by setting V_{GS}=0. When V_{GS}=0, no channel will form under the gate and consequently I_D=0. In order to form a channel, V_{GS} must be greater than the *Threshold Voltage* (V_{Th}). We call this mode the cutoff mode when the voltage $V_{GS} < V_{Th}$ resulting in I_D=0. The value of V_{Th} depends on the doping of the transistor during the manufacturing process and is

typically in the range of 0.3-2.0 V. How much greater V_{GS} is than the V_{Th} is called the excess gate voltage (EGV = V_{GS}-V_{Th}).

$$CUTOFF\ CONDITIONS\text{: } v_{GS} < V_{Th}$$
$$\boldsymbol{CURRENT}\text{: } \quad i_D = 0$$

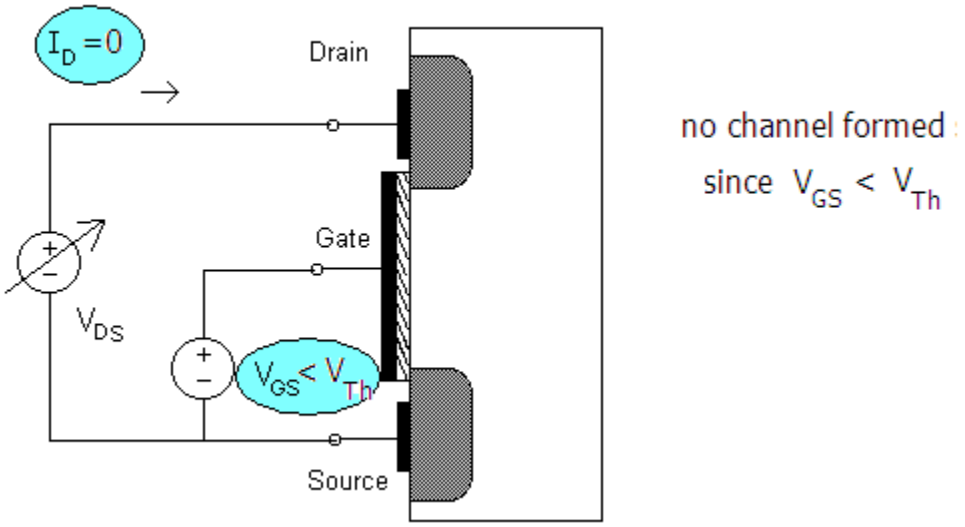


Figure 42: MOSFET in Cutoff

Triode

Triode occurs if V_{GS} is large enough to form a channel and the voltage V_{DS} is relatively small. To continue our experiment, we set V_{GS} so that it is larger than V_{Th}, and we apply a small voltage V_{DS}. Figure 43 shows a MOSFET in triode. Note that the channel that is formed has the same thickness near the drain and source terminals.

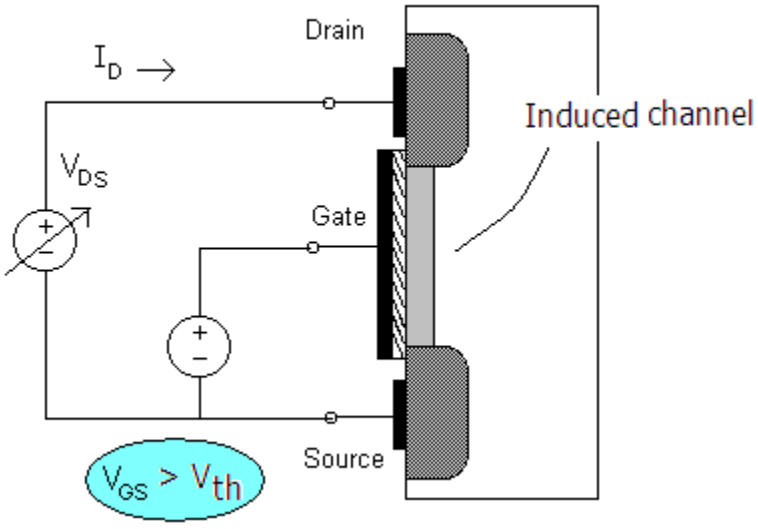


Figure 43: MOSFET in Triode

If we initially set V_{DS}=0 and then gradually increase it, we would find that the drain current increases as V_{DS} increases but then levels off when V_{DS} reaches the excess gate voltage (V_{GS}-V_{Th}). The region before the current levels off is called the triode regions (see Figure 44)

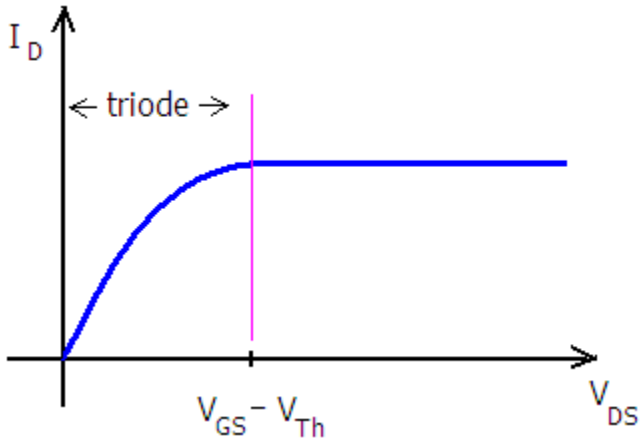


Figure 44: MOSFET I_D vs. V_{DS} for a Single Fixed V_{GS}

If we did this same experiment for other fixed values of V_{GS} above the threshold, and we keep V_{DS} below the excess gate voltage, we would get a family of curves as shown in Figure 45.

Simulation: MOSFET in Triode

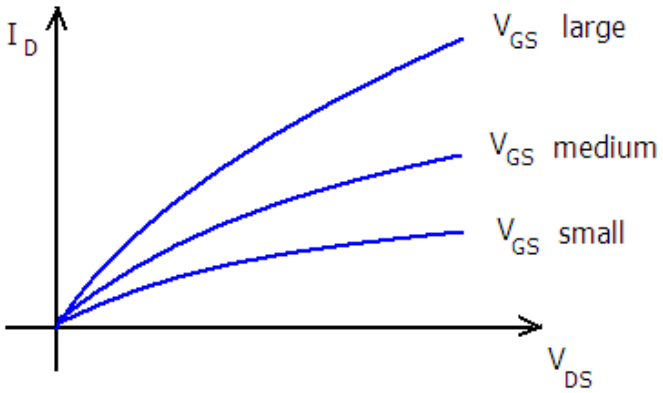


Figure 45: I_D vs. V_{DS} Characteristic for Various Fixed V_{GS}

Note that as long as V_{DS} is relatively small (i.e. $V_{DS} \leq V_{GS}-V_{Th}$) so that the MOSFET remains in the triode region, the current is a function of both V_{DS} and V_{GS}. The triode conditions and the formula for the drain current under triode are given by:

$$\boldsymbol{CURRENT}: \quad i_D = K_n[2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2]$$

$$TRIODE\ CONDITIONS: \quad v_{DS} \leq (v_{GS} - V_{Th}) \ \ AND \ v_{GS} > V_{Th}$$

MOSFETs in triode can function as voltage-controlled resistors. Although not perfectly linear, the I-V characteristic of the MOSFET in triode approximates that of a resistor. The resistance from drain to source is given by:

$$R_{DS} = \frac{\partial v_{DS}}{\partial i_D}$$

If we assume that v_{DS} is small and omit the v_{DS}^2 term, we can write:

$$R_{DS} = \frac{\partial v_{DS}}{\partial i_D} \approx [2K_n(v_{GS} - V_{Th})]^{-1}$$

Note that the voltage V_{GS} controls R_{DS}. Engineers use MOSFETs to make voltage-controlled resistors which combined with operational amplifiers can be used for automatic gain control (AGC) circuits. AGC is useful for equalizing the amplitude of audio signal generated by a microphone from persons located at different distances from the microphone. The ability of a MOSFET to serve as a resistance is also quite useful in integrated circuit design because MOSFETS can be substituted for resistors which require lots of physical space on the chip.

In summary, for the transistor to be in triode, V_{GS} must be sufficiently high to form a channel and V_{DS} must be smaller than the excess gate voltage. The resulting current is a function of both V_{GS} and V_{DS}. The greater the value of V_{GS}, the greater the induced channel depth which in turn results in greater current. We also see that the larger the voltage V_{DS}, the greater the current because this voltage forces current to flow through the channel.

Saturation

We see from Figure 44 that when the voltage V_{DS} is increased beyond V_{GS}-V_{Th}, the current I_D is no longer a function of V_{DS}. At these voltages, the channel becomes non-uniform and limits the amount of current that can flow. For saturation, the current is dependent upon only V_{GS}. (Actually, there is a slight dependence on V_{DS} in saturation but we will leave this discussion for later in the chapter).

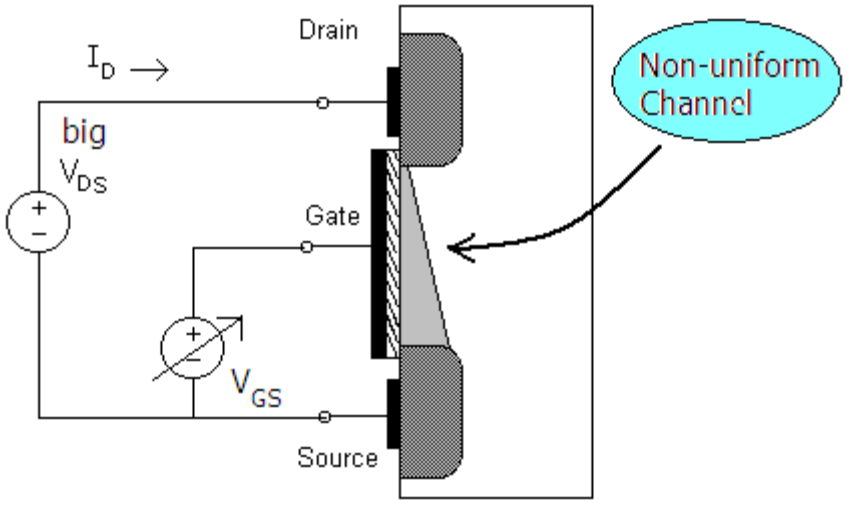


Figure 46: MOSFET in Saturation

To see the effect of V_{GS} on I_D we can vary this voltage and plot the result. We obtain the graph shown in Figure 47 below.

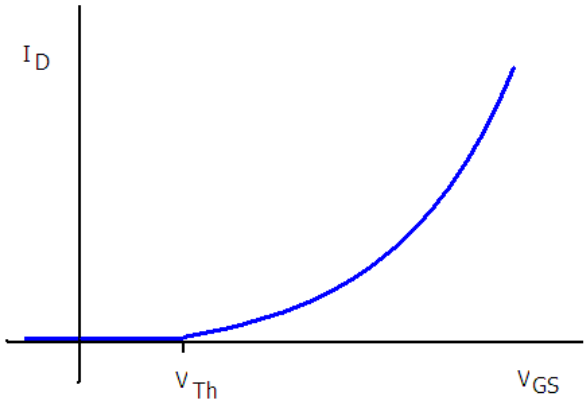


Figure 47: I_D vs. V_{GS}

The transistor functions as a voltage controlled current source in saturation. That is, I_D is controlled by V_{GS}. This property allows the MOSFET to function as an amplifier. The equation for current flow in the saturation region is:

$$\boldsymbol{CURRENT}: \quad i_D = K_n(v_{GS} - V_{Th})^2$$

$$SATURATION\ CONDITIONS: \quad v_{DS} \geq (v_{GS} - V_{Th})\ \ AND\ v_{GS} > V_{Th}$$

In summary, the transistor will be in saturation when V_{GS} is sufficiently high to form a channel and the voltage at the drain is high enough to create a non-uniform channel: $V_{DS} \geq V_{GS} - V_{Th}$. When this occurs, the current is a function of V_{GS} but not V_{DS}.

Simulation: MOSFET Threshold voltage and Regions of Operation

Load Line Analysis and I_D vs. V_{DS} Characteristic Curves

In the previous experiment, we plotted I_D as a function of V_{DS} and V_{GS}. Let's assume that V_{Th} =1.5 V. If we vary V_{DS} for various values of V_{GS} = 2, 3, 4, and 5 V and plot the resulting I_D vs. V_{DS} characteristic curves we would get the graph shown in Figure 48.

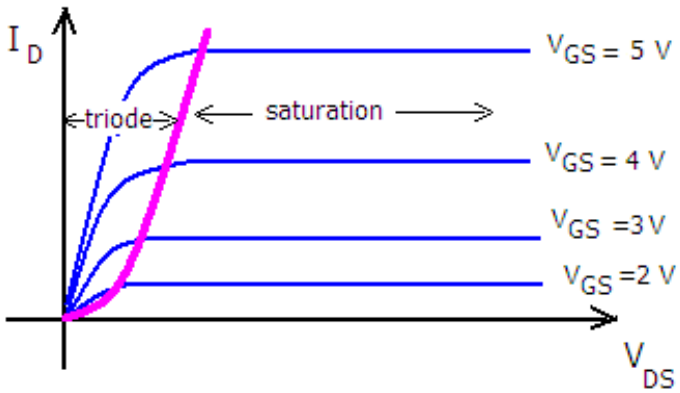


Figure 48: I_D vs. V_{DS} Curves for various V_{GS}

We will find that this plot is quite useful in performing load line analysis.

For the circuit shown in Figure 49, we will draw the load line on the i_D vs. v_{DS} characteristic plot as shown in Figure 50. We see that if V_G= 2 V, the operating point is in the saturation region. If V_G=5 V, the operating point is in the triode region. We will see later that for amplifier applications, we want the MOSFET to operate in the saturation region. For switching applications, the triode region is usually desirable. From the load line, we can also see how altering R_D and V_{DD} affects operating region. For instance, if V_G=5 V and we wanted the transistor to be in the saturation region, we could either increase V_{DD} or decrease the resistance R_D.

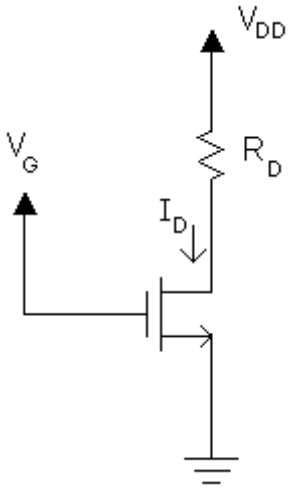


Figure 49: MOSFET Circuit to Investigate Load Line Analysis

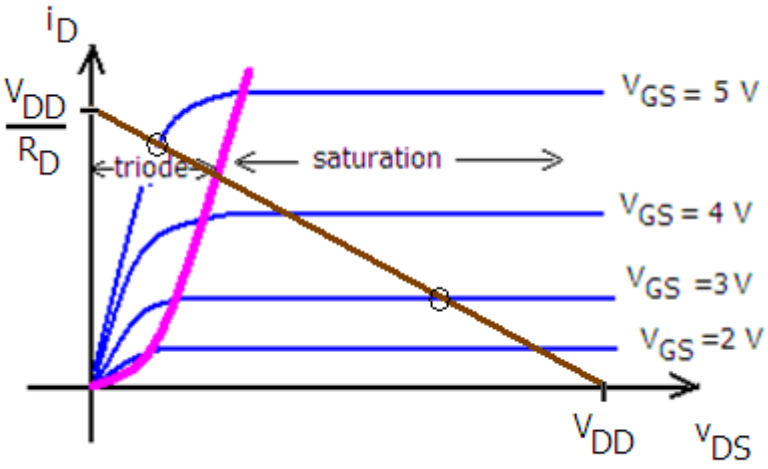


Figure 50: Load Line on Characteristic Curves

Example 1: MOSFET in Saturation

Determine the mode of operation and the drain current I_D for a MOSFET with K_n=1 mA/V^2, V_{Th}=1 V, V_{GS}=3 V and V_{DS}=7 V.

Since $V_{GS}>V_{Th}$ and $V_{DS} \geq (V_{GS}-V_{Th})$ the transistor is in **saturation**. Therefore:

$$i_D = K_n(v_{GS} - V_{Th})^2$$
$$i_D = 1 \times 10^{-3}(3-1)^2$$
$$i_D = 4\,mA$$

Example 2 : MOSFET in Triode

Determine the mode of operation and the drain current I_D for a MOSFET with K_n=1 mA/V^2, V_{Th}=1 V, V_{GS}=3 V and V_{DS}=0.5 V.

Since $V_{GS}>V_{Th}$ and $V_{DS} \leq (V_{GS}-V_{Th})$ the transistor is in **triode**. Therefore:

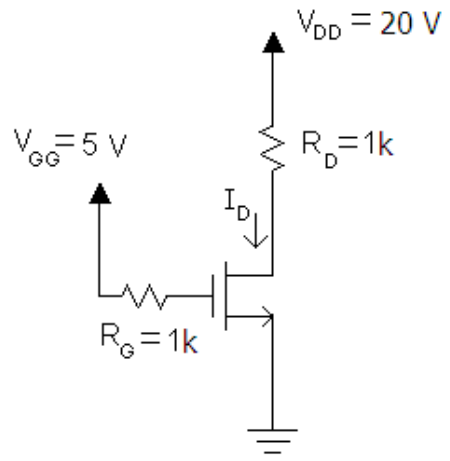
$$i_D = K_n[2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2]$$
$$i_D = (1 \times 10^{-3})[2(3-1)0.5 - 0.5^2]$$
$$i_D = 1.75\,mA$$

NMOS DC Circuits

We will now analyze circuits containing NMOS transistors. As we did with diode circuits, we will assume an operating region. The operating region determines which equation is used to determine the drain current I_D. Once the drain current is determined, we can calculate the voltages V_{GS} and V_{DS} to see if they place the transistor in the assumed operating region. If the assumed operating region is confirmed, the analysis is complete. If not, we must reanalyze the circuit using a different assumption. In the case of diodes, we replaced the diode with circuit models such as an open circuit, short circuit, or voltage source depending on the model used and the operating region assumed. For MOSFETs, we will not be using circuit models; rather we will use the equations relating the terminal parameters. This is similar to the approach we used when employing the Shockley equation with diodes.

Example 3: MOSFET DC Circuit

Determine the drain current in the circuit below. Assume K_n=0.5 mA/V^2 and V_{Th}=1 V,



We first note that V_G=5 V because there is no voltage drop across R_G since no current flows into or out of the gate terminal. We also note that the source is grounded (V_S=0) and therefore V_{GS}=5 V. Since $V_{GS}>V_{Th}$, the transistor must be in either the triode or saturation region. We will assume the transistor is in saturation. For saturation:

$$I_D = K_n(V_{GS} - V_{Th})^2$$
$$I_D = 0.5 \times 10^{-3}(5-1)^2$$
$$I_D = 8\,mA$$

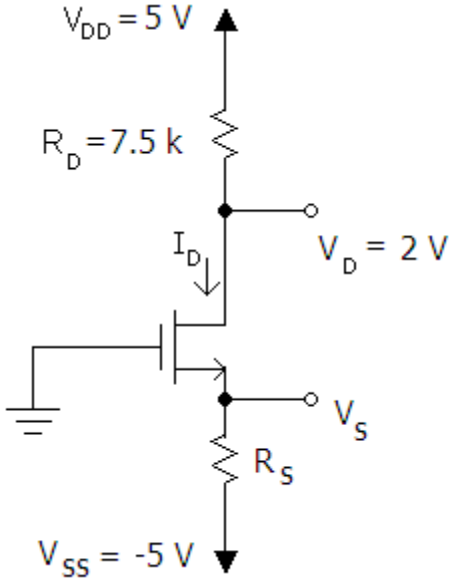
Next, we calculate V_{DS} to determine if our assumption of saturation mode is correct.

$$V_D = V_{DD} - R_D \times I_D$$
$$V_D = 20 - 1k \times 8m$$
$$V_D = 12\,V$$

Because the source is grounded, $V_{DS}=V_D$=12 V. Since $V_{DS} \geq V_{GS}-V_{Th}$ our assumption is correct.

Example 4: MOSFET DC Circuit

Determine I_D, V_S, and R_S. Assume V_{Th}=1 V, k'=20 µA/V, W=400 µm, and L=10 µm. V_D=2 V.



We first solve for the current I_D:

$$I_D = \frac{V_{R_D}}{R_D} = \frac{(5-2)}{7.5k} = 0.4\text{ mA}$$

Next, we calculate K_n:

$$K_n = \frac{1}{2}k'\frac{W}{L} = \frac{1}{2}20\mu\frac{400\mu}{10\mu} = 0.4\,mA/V^2$$

Assuming saturation:

$$i_D = K_n(v_{GS} - V_{Th})^2$$
$$0.4m = 0.4m(V_{GS} - 1)^2$$

$$V_{GS} = \cancel{0\,V}\ or\ 2\,V$$

We reject the first root because V_{GS}=0V would place the MOSFET in cutoff. The voltage V_S can be calculated since we know both V_{GS} and V_G:

$$V_{GS} = V_G - V_S$$

$$V_S = V_G - V_{GS}$$
$$V_S = 0 - 2$$
$$V_S = -2\,V$$

Next, we calculate V_{DS} from:

$$V_{DS} = V_D - V_S$$

$$V_{DS} = 2 - (-2) = 4\,V$$

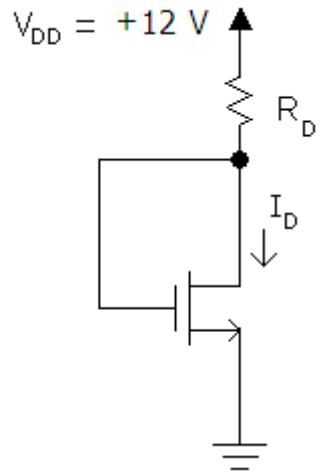
Since $V_{DS} \geq V_{GS} - V_{Th}$ the MOSFET is indeed in saturation. Finally, we calculate R_S.

$$R_S = \frac{V_{R_S}}{I_D} = \frac{(-2 - (-5))}{0.4\text{m}} = 7.5\ \text{k}\Omega$$

Answers: I_D=0.4 mA, V_S = -2 V, and R_S=7.5 kΩ

Example 5: MOSFET Circuit Design Problem

Design the circuit below so that I_D=0.8 mA. Assume that k'=20 μA/V^2, L=10 μm, W=200 μm, and V_{Th}=2 V.



First we calculate the transistor parameter K_n.

$$K_n = \frac{1}{2} k' \frac{W}{L}$$

$$K_n = \frac{1}{2} 20\mu \frac{200\mu}{10\mu} = 0.2\ mA/V^2$$

Since V_{DS}=V_{GS} the transistor must be in saturation.

$$i_D = K_n (v_{GS} - V_{Th})^2$$

We note that because the source voltage is grounded (Vs=0), $V_{GS}=V_{DS}=V_D$. Substituting into the saturation equation yields:

$$0.8 = 0.2(V_D - 2)^2$$

$$V_D = \cancel{0\,V}\ or\ 4\ V$$

Since V_D=0 V would result in cutoff we can eliminate this solution. We now calculate R_D using Ohm's law:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$I_D = \frac{12 - 4}{0.8} = 10\ k\Omega$$

Simulation of MOSFET Circuits

There are several simulation tools available to simulate MOSFET circuits including PSPICE, the Java Circuit Simulator, and many others. Because the Java Circuit Simulator is easy to use and many simulation examples are presented in this text, we will briefly examine how to simulate MOSFET circuits with this tool. If you right click the MOSFET circuit element, there are two parameters that can be specified: the threshold voltage and beta. The threshold voltage is self-explanatory, the beta value is equal to k'W/L. Therefore:

$$Beta = 2K_n$$

When using the Java Circuit Simulator simply specify these values and you will be able to simulate all of the MOSFET DC circuit examples in this text.

Simulation: DC Circuit Example

MOSFET as a Switch

Discrete power MOSFETs are often used for switching applications where the MOSFET acts as a voltage-controlled switch. Power MOSFETs employ semiconductor processing techniques that are similar to those of integrated circuits (IC), although the device geometry, voltage and current levels are significantly different from the design used in ICs. The development of the power MOSFET was partly driven by the limitations of bipolar power junction transistors (BJTs) which, until recently, were the device of choice in power electronics applications.

A power MOSFET would be useful in applications where a microcontroller is being used to control a motor. In the circuit shown in Figure 51, the microcontroller's output pin is being used to switch on and off a motor. The MOSFET is used because the microcontroller cannot source the required current. Also, microcontroller voltage outputs are typically limited to 5 V maximum where in the application below, the motor voltage is 10 V.

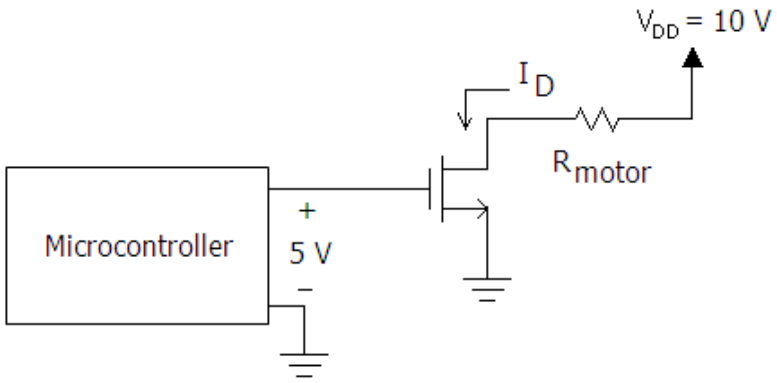


Figure 51: MOSFET as Switch

In addition to activating a motor, the microcontroller in conjunction with the MOSFET can perform speed control. By switching the MOSFET on and off very quickly (typically hundreds of times per second) the speed of the motor can be controlled. This method of speed control is called pulse width modulation (PWM). The percentage of time the motor is switched on is called the duty cycle and by controlling the duty cycle, the microcontroller can control the speed of the motor. For instance, a duty cycle of 30% means that the MOSFET "switch" is closed 30% of the time. A graph illustrating the concept of duty cycle is shown in Figure 52.

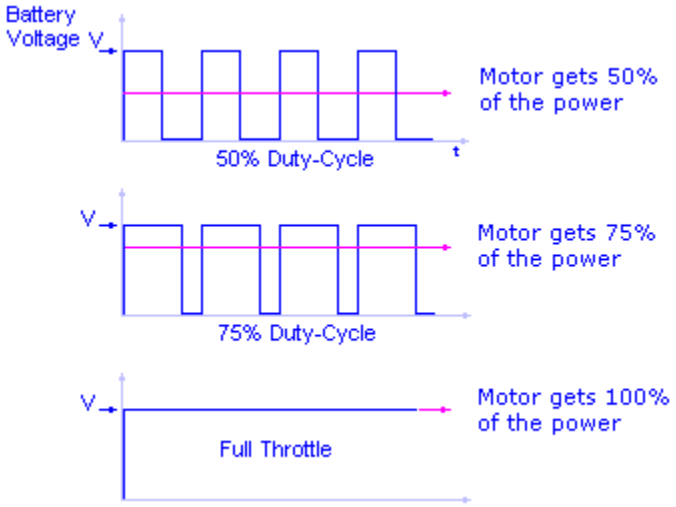


Figure 52: Duty Cycle

Simulation: Controlling a Motor Using a MOSFET

Example 6: MOSFET Used as a Switch to Control a Motor

For the power MOSFET circuit shown in Figure 51, determine I_D when the microcontroller output is 5 V. Assume V_{Th}=2 V, K_n=50 mA/V^2, and R_{motor}=100 ohms.

Although it seems likely that the MOSFET would be in triode, we will begin with the assumption that the MOSFET is in saturation. We do this to illustrate that incorrect initial assumptions can be checked and corrected.

$$i_D = K_n(v_{GS} - V_{Th})^2$$
$$i_D = 50m(5-2)^2 = 0.45\ A$$

Therefore, since V_S=0 we can calculate V_{DS} using KVL as follows:

$$V_{DS} = V_{DD} - R_D \times I_D$$
$$V_{DS} = 10 - 100 \times 0.45 = -35\ V$$

Note that V_{DS}<V_{GS}-V_{TH}. Therefore, the saturation assumption is invalid. For Triode:

$$i_D = K_n[2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2]$$
$$I_D = 50m[2(5-2)V_{DS} - V_{DS}^2]$$

The current can be found using KVL:

$$I_D = \frac{10 - V_{DS}}{100}$$

If we set the two previous equations equal to each other and solve for V_{DS} using the quadratic equation, we obtain the following roots:

$$V_{DS} = 0.341\ V\ or\ = \sout{5.86\ V}$$

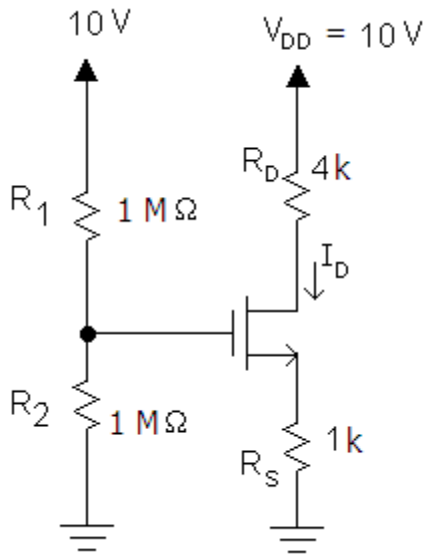
Note that the last root is impossible as this would place the transistor in saturation. Therefore, V_{DS} = 0.341 V which results in I_D = 96 mA. If the MOSFET were a perfect switch (i.e. zero voltage drop across the switch) we would obtain I_D = 100 mA. Therefore, the MOSFET does a good job of acting as a switch and very little power is wasted in the MOSFET. Another way to think about this is that the resistance from source to drain is quite low resulting in very little voltage drop across the MOSFETs terminals. Note that the microcontroller output requirements are minimal as the microcontroller is not required to source any current. This is a major advantage over the Bipolar Junction Transistor (BJT).

Bias Circuits for MOSFET Amplifiers

Bias circuits are used to place the transistor in a particular region of operation. For amplifiers, the saturation region is used. We will investigate several common bias circuits before turning our attention to amplifier analysis.

Example 7: Analysis of a Four Resistor Bias Network

Determine I_D. Assume V_{Th}=2 V, K_n=0.25 mA/V^2. This circuit is commonly used as a bias circuit for amplifiers.



We first note that R1 and R2 form a voltage divider because the gate current is zero. Therefore V_G=5 V. We can write the voltage V_{GS} as:

$$V_{GS} = V_G - V_S$$
$$V_{GS} = 5 - 1k \times I_D$$

$$i_D = K_n(v_{GS} - V_{Th})^2$$
$$I_D = 0.25\big((5 - 1 \times I_D) - 2\big)^2$$
$$4I_D = (3 - 1I_D)^2$$
$$(I_D)^2 - 10I_D + 9 = 0$$
$$I_D = 1\ mA\ or\ \sout{9\ mA}$$

I_D=9 mA cannot be a root because V_S=9V which results in V_{GS} = -4 V which would place the MOSFET in cutoff. Therefore I_D= 1 mA. Next, we calculate V_{DS}.

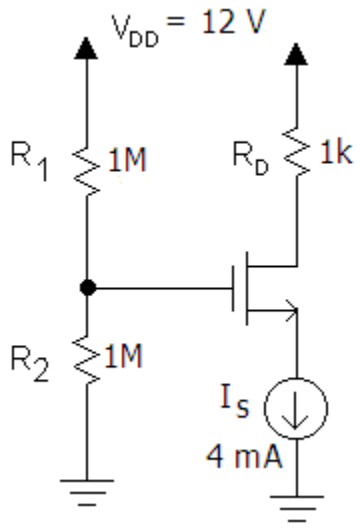
$$V_S = 1k \times I_D = 1\ V$$
$$V_D = V_{DD} - R_D \times I_D = 10 - (4k)(1m) = 6\ V$$
$$V_{DS} = V_D - V_S = 5\ V$$

Since $V_{DS} \geq V_{GS} - V_{Th}$ saturation assumption is valid.

Answer: I_D = 1 mA.

Example 8: Bias Circuit with Current Source

Determine the voltage V_S in the circuit below. Assume that K_n=1 mA/V^2 and V_{Th}=1 V.



The drain current I_D=I_S=4 mA. Using voltage division, we determine that:

$$V_G = 12\left(\frac{1M}{1M + 1M}\right) = 6\,V$$

The voltage V_D can be determined from KVL:

$$V_D = 12 - 4m \times 1k = 8\,V$$

Assuming saturation region, we determine the voltage V_{GS}.

$$I_D = K_n(V_{GS} - V_{Th})^2$$

$$V_{GS} = \sqrt{\frac{I_D}{K_n}} + V_{Th}$$

$$V_{GS} = \sqrt{\frac{4}{1}} + 1$$

$$V_{GS} = 3\,V$$

We find the voltage at the source terminal as follows:

$$V_S = V_G - V_{GS}$$

$$V_S = 6 - 3 = 3\,V$$

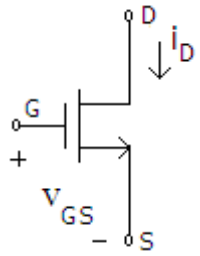
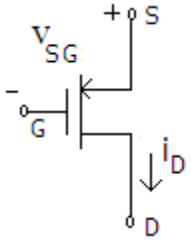
Since $V_{DS} \geq (V_{GS}-V_{Th})$ and $V_{GS}>V_{Th}$, the transistor is in the saturation region as assumed.

PMOS Transistors at DC

PMOS transistors use p-type material rather than n-type material to form the channel from drain to source. The characteristics of p-channel MOSFETs are the same as for n-channel MOSFETS

except that the voltage polarities and current directions are inverted. The schematic symbol for a p-channel device is shown below.

To form a channel the gate must be below the source voltage by at least V_{Th} volts (V_{Th} is negative for PMOS). In other words, to form a channel, $V_{SG} > |V_{Th}|$. Assuming a channel is formed, to operate the transistor in saturation the source voltage V_S must not drop below the drain voltage by more than $|V_{Th}|$ volts.

	NMOS (enhancement mode)	PMOS(enhancement mode)
Schematic Symbol		
Cutoff	$v_{GS} \leq V_{Th}$ $i_D = 0$	$v_{SG} \leq \|V_{Th}\|$ $i_D = 0$
Triode	$v_{DS} \leq (v_{GS} - V_{Th})\ \ AND\ v_{GS} > V_{Th}$ $i_D = K_n[2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2]$	$v_{SD} \leq (v_{SG} - \|V_{Th}\|)\ \ AND\ v_{SG} > \|V_{Th}\|$ $i_D = K_n[2(v_{SG} - \|V_{Th}\|)v_{SD} - v_{SD}^2]$
Saturation	$v_{DS} \geq (v_{GS} - V_{Th})\ \ AND\ v_{GS} > V_{Th}$ $i_D = K_n(v_{GS} - V_{Th})^2$	$v_{SD} \geq (v_{SG} - \|V_{Th}\|)\ \ AND\ v_{SG} > \|V_{Th}\|$ $i_D = K_p(v_{SG} - \|V_{Th}\|)^2$

Example 9: PMOS Regions of Operation

Determine the region of operation for a PMOS transistor with a V_{Th}= -1 V operating with the following conditions:

a. V_{SG}=2 V and V_{SD}=0.5 V
b. V_{SG}=2 V and V_{SD}=3.5 V
c. V_{SG}=0.5 V and V_{SD}=5.0 V

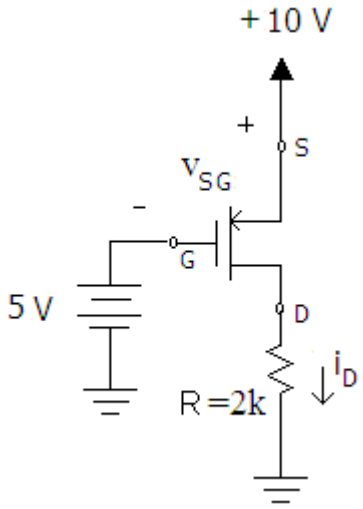
For part a: Since $V_{SG}>|V_{Th}|$ the transistor is either in triode or saturation. The transistor is operating in the triode region because $V_{SD} \leq (V_{SG} - |V_{Th}|)$.

For part b: Since $V_{SG}>|V_{Th}|$ the transistor is either in triode or saturation. The transistor is operating in the saturation region because $V_{SD} \geq (V_{SG} - |V_{Th}|)$.

For part c: Since $V_{SG}<|V_{Th}|$ the transistor is in cutoff.

Example 10: PMOS DC Circuit Analysis

Determine the current i_D in the transistor circuit below. Assume that K_p=0.25 mA/V^2 and V_{Th}= -1 V.



First we make sure that the transistor is not in cutoff (i.e. the source to gate voltage is sufficiently high to form a channel).

$$v_{SG} > |V_{Th}| \, ?$$

$$(10 - 5) > |-1| \, ?$$

$$yes, so\ the\ transitor\ is\ in\ either\ triode\ or\ saturation.$$

We will assume that the transistor is operating in the saturation region and then check the assumption for validity. For saturation:

$$i_D = K_p(v_{SG} - |V_{Th}|)^2$$

$$i_D = 0.25m(5 - |-1|)^2$$

$$i_D = 4\ mA$$

Therefore V_D= 8V which results in V_{SD}=2V. But for saturation:

$$V_{SD} \geq (V_{SG} - |V_{Th}|)$$

$$2 \geq (5 - |-1|) \text{ NOT TRUE!}$$

Therefore, the transistor is in triode. Note that $v_{SD} = v_S - v_D = 10 - 2ki_D$.

$$i_D = K_p[2(v_{SG} - |V_{Th}|)v_{SD} - v_{SD}^2]$$

$$i_D = 0.25m[2(5 - |-1|)(10 - 2ki_D) - (10 - 2ki_D)^2]$$

$$i_D = \sout{1.38\ mA}\ \ or\ \ = 3.62\ mA$$

We can reject the first root since for triode $V_{SD} \leq (V_{SG} - |V_{Th}|)$.

Logic Circuits

MOSFETs are commonly used in logic circuits. By combining MOSFETs, all types of logic gates can be constructed. Typically, logic circuits use 0 V to represent logic 0 and 5 V to represent logic 1. Like the motor driver circuit discussed previously, the MOSFET is biased to act as a switch using the cutoff and triode modes. For cutoff, the MOSFET is an open circuit. In triode, the MOSFET approximates a short circuit because V_{DS} is small.

The simplest logic circuit is the inverter shown in Figure 53 below. A logic inverter will produce a low signal when the input is high, and vice versa.

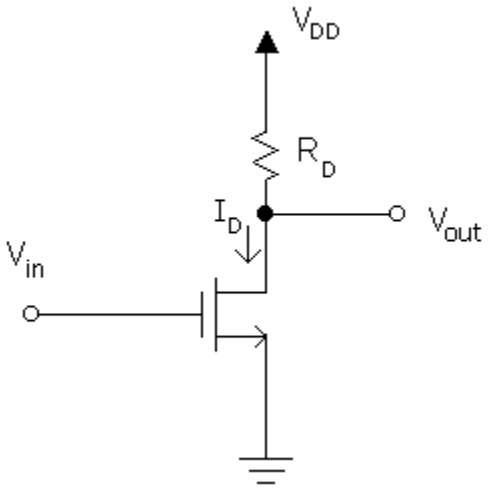


Figure 53: Logic Inverter

When V_{in} is below the threshold voltage, there will be no channel formed and consequently I_D=0. This condition will result in V_{out}=V_{DD} because there will be no voltage drop across resistor R_D. As V_{in} increases, the transistor will be in the saturation mode and V_{out} will decrease as the drain current increases due to the voltage drop across R_D. As V_{in} increases still further, the voltage V_D (which equals V_{DS}) will continue to drop until V_D is less than V_G-V_{Th} and the MOSFET enters triode.

The resulting transfer characteristic plot is shown in Figure 54. Increasing the value of R_D will result in a larger voltage drop across R_D which will cause the MOSFET to enter the triode region at a smaller value of V_{in}.

Simulation: Logic Inverter

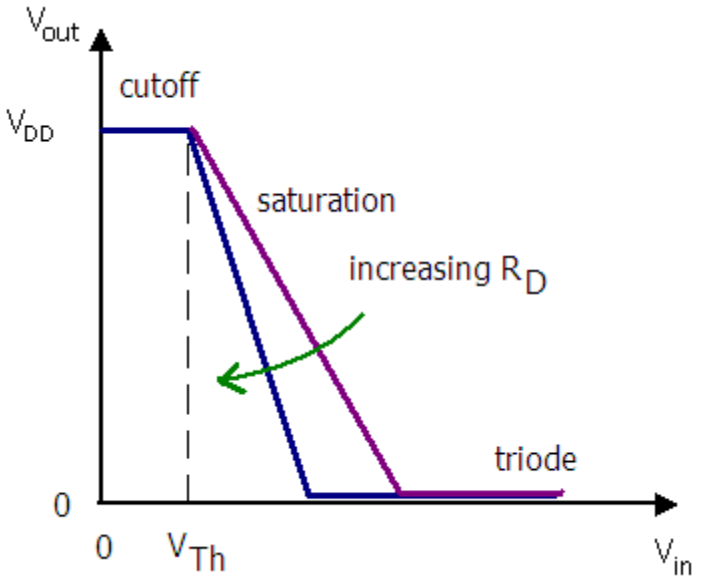
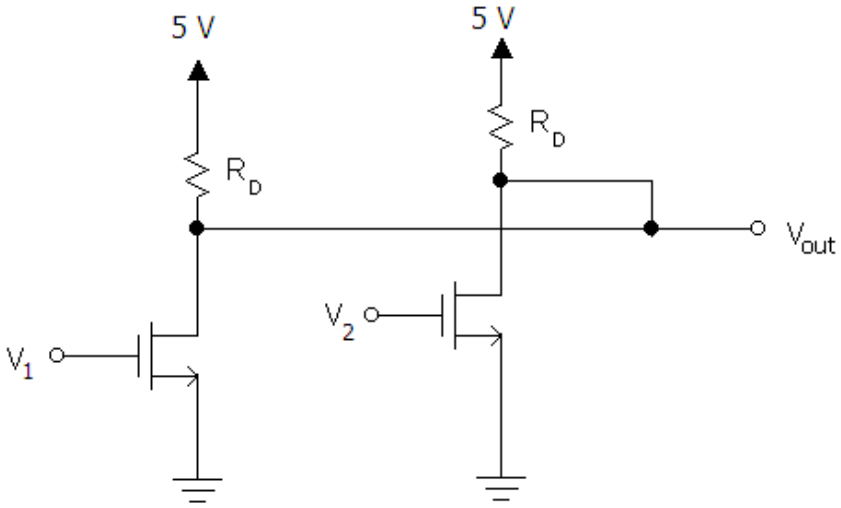


Figure 54: Inverter Transfer Characteristic

The circuit in Figure 55 represents the logic NOR (OR but with the output inverted). The output is low if either of the inputs is low; otherwise, the output voltage is approximately equal to 5 V (this assumes that R_D is sufficiently high for the transistor to be in triode when the transistor gate voltage is high.



V_1	V_2	V_{out}
0	0	5 V
0	5 V	0
5 V	0	0
5 V	5 V	0

Figure 55: Logic NOR Circuit

Simulation: NOR Gate Circuit

Current Mirrors

Next, we show how matched transistors can be used to construct current sources. These current sources can be used to bias amplifiers – especially those on integrated circuits.

Figure 56 shows a current mirror configuration. Because the $V_G=V_D$, the transistor must be biased in the saturation region (assuming $V_{DD}>V_{Th}$). Note that because the gate terminals of each of the MOSFETS are tied together, $V_{GS0}=V_{GS1}=V_{GS2}$. If we assume that the MOSFETs are identical, the currents produced by M1 and M2 will equal I_{ref} (remember that no current flows in or out of the gate). Therefore, we can choose R_D to establish the desired reference current I_{ref}, and this reference current is "mirrored" to I_1 and I_2. Using this technique, many identical current sources can be produced on an IC. We can alter the values of the mirrored current sources by altering the W/L ratio of these transistors. The current mirror configuration works as long as each of the transistors operates in the saturation region. If the load placed above M1 is too large, the drain to source voltage will drop and take the transistor out of the saturation region and therefore I_1 would not equal I_{ref}.

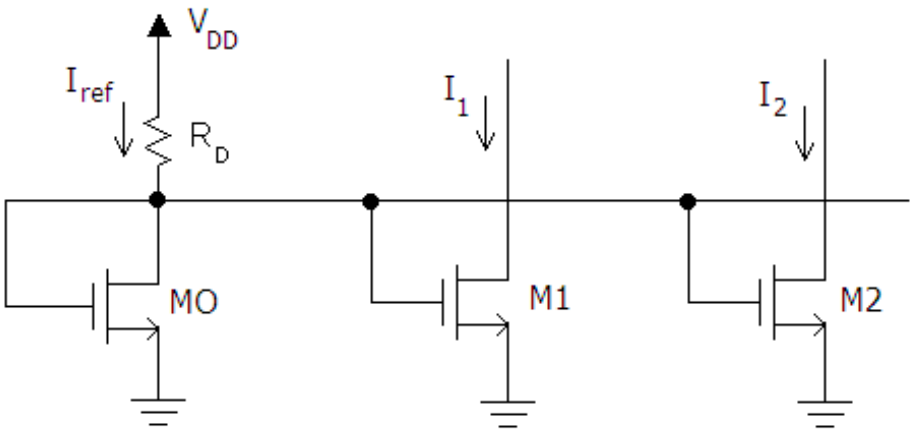


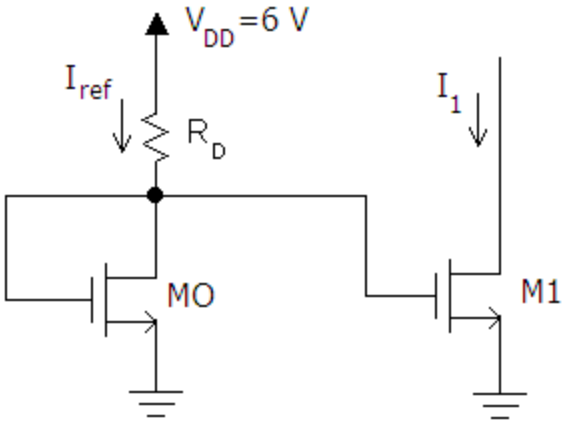
Figure 56: Current Mirror

Simulation: Current Mirror

Example 11: Current Mirror Design

Refer to the figure below. Assume the $K_{n1}=K_{n2}=1$ mA/V^2, $V_{Th1}=V_{Th2}=1$ V, and $V_{DD}=6$ V.

a. Design a current mirror source that produces $I_1=10$ mA.
b. Determine the largest load resistor that could be placed above M1 if the value of V_{DD} for that transistor is 6 V.



Solution for part a

Since the transistors are identical, $I_{ref}=I_1=10mA$. We must choose R_D so that it produces $I_{ref}=10$ mA. Using the saturation equation for the transistor:

$$10m = 1m(v_{GS} - 1)^2$$
$$v_{GS} = 4.16\,V$$

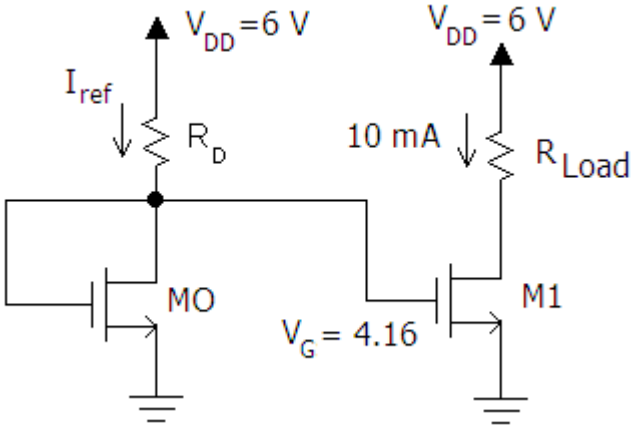
Note that $V_D = V_G = V_{GS}$. Therefore:

$$R_D = \frac{6 - 4.16}{10m} = 184\ \Omega$$

Using this value of R_D will produce a current $I_1=10$ mA.

Solution for part b

The schematic for this scenario is shown below.



For saturation V_D must be greater or equal to V_G-V_{Th}. Therefore, the minimum value for $V_D=3.16$ V. Using ohms law to calculate R_{LOAD} yields:

$$R_{Load} = \frac{6 - 3.16}{10m} = 284\ \Omega$$

R_{Load} must be less than or equal to 284 Ω for M1 to remain in saturation and maintain a current of 10 mA.

Amplifiers

An important application of MOSFETs is the amplification of signals. MOSFETs can be used to amplify voltages, currents, or both. Because typical MOSFET amplifiers are biased to operate in the saturation region, we will assume this to be the case in the discussion that follows. We will begin by looking at MOSFET amplifiers using a load line approach which provides a qualitative introduction to MOSFET amplifiers. We then develop the small signal model that will allow us to analyze more complicated practical amplifier circuits.

We will illustrate that MOSFETs can be used to amplify signals using the "conceptual amplifier" circuit shown in Figure 57. (It is not a good "real" circuit because it requires two power supplies to bias the MOSFET)

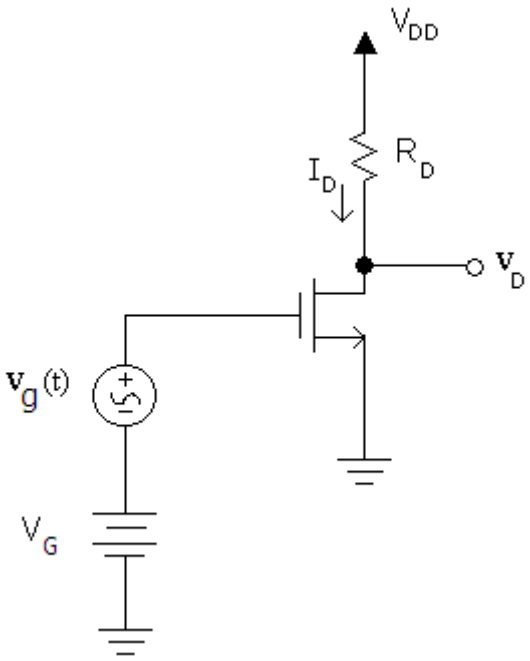


Figure 57: Conceptual Amplifier Circuit

We will assume that the amplifier is biased to operate in the saturation region by the voltage sources V_G and V_{DD}. The input signal to be amplified is v_g. The output of the amplifier is taken at the drain v_D.

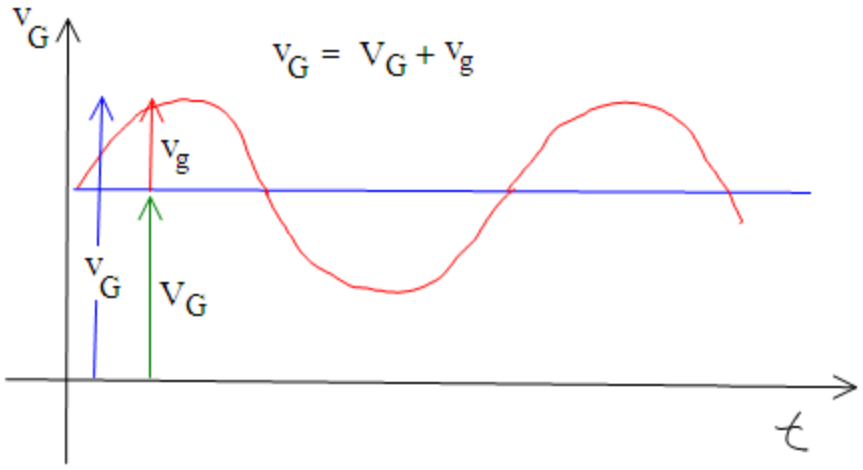


Figure 58: Total, DC, and Small Signal Quantities

As seen from Figure 58, the total gate voltage v_G consists of the dc voltage V_G and the time varying voltage v_g. Using the subscript convention introduced previously for small signal analysis: $v_G=V_G+v_g$. The signal v_g will cause the voltage at the gate v_G to fluctuate over time. As the gate voltage increases, the current i_D will increase which causes the voltage at the drain to decrease because of the greater voltage drop across R_D. When the voltage at the gate decreases, the current i_D decreases and the voltage at the drain will go up. How much the drain voltage goes up and down is dependent upon K_n, R_D, and the V_G. Because the drain voltage decreases when v_g increases and vice versa, the amplifier is said to be inverting. If all this seems confusing, read this paragraph over a few more times and it should become clearer.

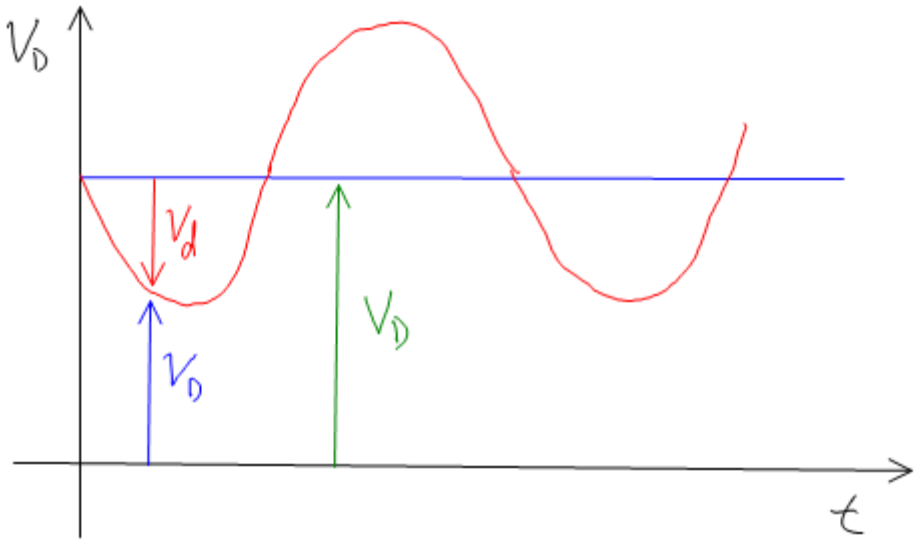
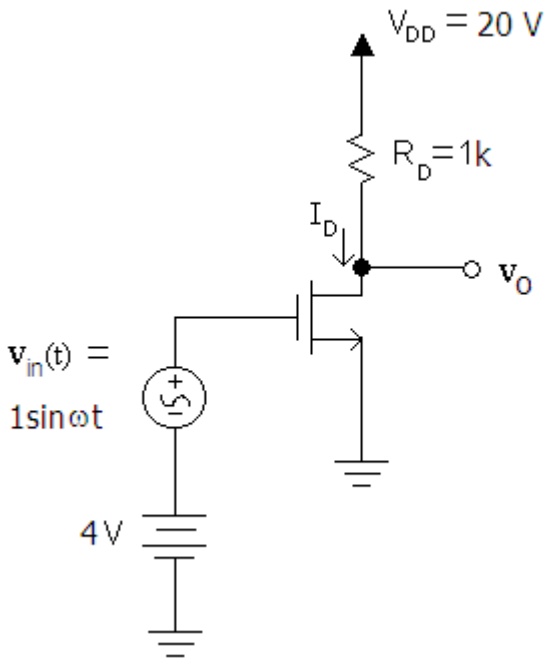


Figure 59: Conceptual Amplifier Output

We continue our qualitative examination of the amplifier using load line analysis.

Example 12: Load Line Analysis of an Amplifier

Perform load line analysis to determine the maximum and minimum voltage v_o and the voltage gain (A_V).

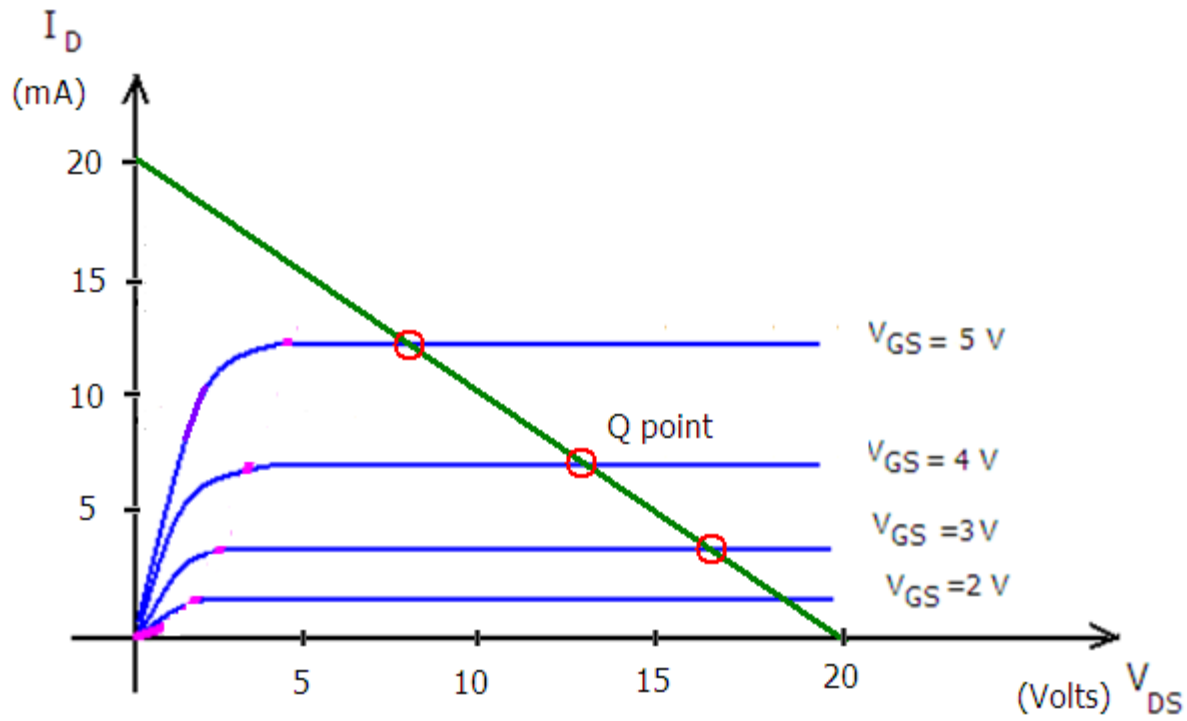


The voltage at the gate (v_G=4+1sinωt V) will vary from 3 to 5 V. Since the source is tied to ground, the voltage v_{GS} will also vary from 3 to 5 V. The load line equation can be found using KVL:

$$V_{DS} = V_{DD} - R_D \times I_D$$

$$V_{DS} = 20 - 1k \times I_D$$

We plot this equation on the i_D vs. v_{DS} characteristic plot of the MOSFET (see figure below). The Q point is when $v_{in}(t)=0$. The maximum and minimum values for v_{DS} (which is the same as v_o) occur when v_{GS} is at its maximum and minimum values. The minimum value for V_{GS} is 3 V.



The characteristic curve for V_{GS}=3 V intersects the load line at v_o≈17 V. For V_{GS}=5 V the result is v_0≈8 V. At the Q point, v_o≈13 V. Note that as v_{in} varies by 2 V, the output voltage v_o varies by 9 V. The voltage gain therefore is:

$$A_V = \frac{\Delta v_o}{\Delta v_{in}} = \frac{-9}{2} = -4.5\ \frac{V}{V}$$

Although the gain A_V is a dimensionless quantity, it is customary to use V/V as the unit to emphasize that the result is a voltage gain. The gain is negative because the amplifier inverts the input signal; as v_{in} increases from 3 to 5 V, the output voltage decreases from 17 to 8 V.

Load line analysis is helpful to understand how amplifiers work; however, it is an inconvenient method to calculate gain. We now turn to small signal analysis to calculate gain and other amplifier characteristics.

Simulation: Simple MOSFET Amplifier

Small Signal Model

Using small signal analysis we can calculate amplifier characteristics such as voltage gain, current gain, input resistance and output resistance in a systematic way. As we found with diodes, small signal analysis looks at how a circuit responds to small changes. In order to perform small signal analysis, we must have a circuit model – called the small signal model – that describes how a MOSFET responds to small changes. For instance, we found that a diode can be modeled as a resistance for small signals. We start the development of the small signal model of the MOSFET by referring to its I-V characteristics in saturation. We are interested in

saturation since that is the typical operating mode for MOSFET amplifiers. The saturation equation and the resulting graph are repeated below.

$$i_D = K_n(v_{GS} - V_{Th})^2$$

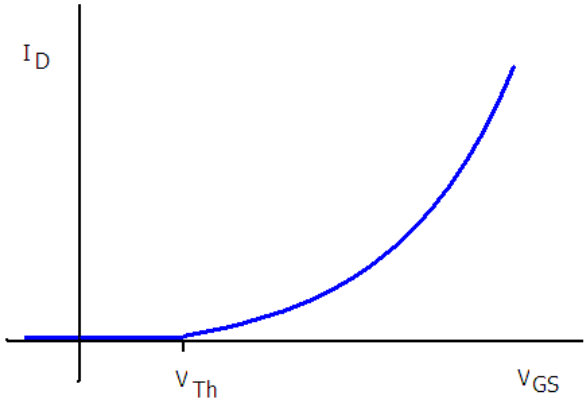


Figure 60: I_D vs V_{GS}

In our qualitative examination of a MOSFET amplifier circuit we found that changes in the gate voltage created changes in the drain current. We found that we could get the MOSFET to amplify signal by biasing the transistor in the saturation region using a DC source and applying the input signal in series with the DC source as shown in Figure 61 below.

$$v_{GS}=V_{GS}+v_{gs}$$

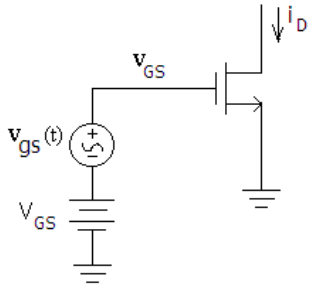


Figure 61: Small Signal in Series with Gate Bias Voltage

In Figure 62 below, the Q point is shown as V_{GSQ} and I_{DQ}. The instantaneous operating point moves up and down the curve over time because of $v_{gs}(t)$. If we assume that magnitude of $v_{gs}(t)$ is small, the curve can be approximated as a straight line corresponding to the slope at the Q point.

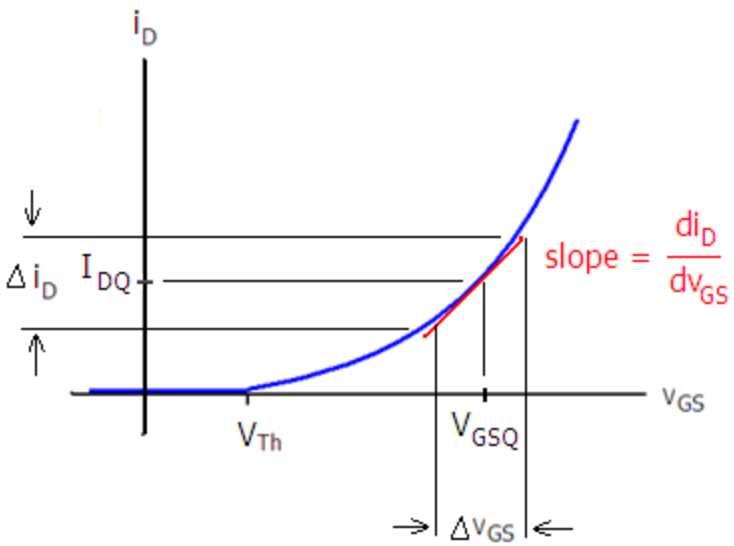


Figure 62: Small Signal Approximation

The slope of the curve at the DC operating point or Q-point is:

$$slope = \left.\frac{di_D}{dv_{GS}}\right|_{Q\ point}$$

For small Δv_{GS} we can write:

$$slope = \left.\frac{di_D}{dv_{GS}}\right|_{Q\ point} \approx \frac{\Delta i_D}{\Delta v_{GS}}$$

The slope of the line at the Q point is called the transconductance. The name transconductance derives from the fact that the slope has units of conductance and that it relates the voltage at one set of terminals to the current at another (transfer). We define the transconductance g_m as:

$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_{Q}$$

For small changes:

$$\Delta i_D \approx g_m \Delta v_{GS}$$

Since Δv_{GS} represents the small signal voltage (v_{gs}) and Δi_D represents the small signal current we can write:

$$i_d \approx g_m v_{gs}$$

We can represent the equation above with the small signal equivalent circuit shown in Figure 63. The gate to source terminals are open circuited because the small signal gate current is zero.

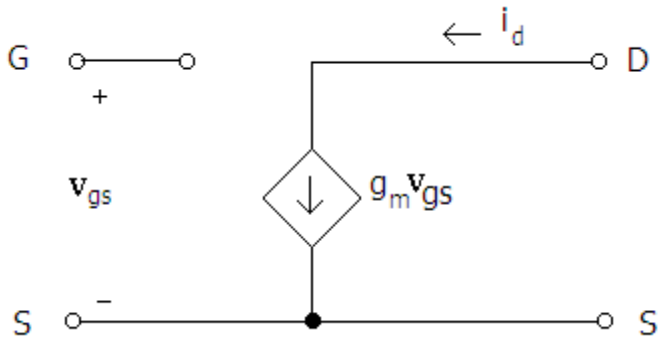


Figure 63: MOSFET Small Signal Model

The small signal model of the MOSFET shows that the small signal drain current i_d is dependent upon the small signal gate to source voltage v_{gs}. The MOSFET acts as a linear voltage controlled current source for small signals. In actuality, the relationship is non-linear, but we have approximated the relationship as linear for small signals. As the instantaneous operating point of moves further from the Q-point, the approximation becomes worse.

Now we turn our attention to finding the transconductance parameter g_m. For saturation:

$$i_D = K_n(v_{GS} - V_{Th})^2$$

To find g_m we take the derivative of this equation with respect to v_{GS} at the Q point:

$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_{Q\ point} = 2K_n(v_{GS} - V_{Th})|_{Q\ point}$$

The Q point occurs when v_{GS}=V_{GSQ} therefore:

$$g_m = 2K_n(V_{GSQ} - V_{Th})$$

We can also derive an equation for g_m in terms of the quiescent drain current I_{DQ}.
Since:

$$I_{DQ} = K_n\left(V_{GSQ} - V_{Th}\right)^2$$

Then

$$\sqrt{\frac{I_{DQ}}{K_n}} = \left(V_{GSQ} - V_{Th}\right)$$

We can therefore write:

$$g_m = 2\sqrt{K_n I_{DQ}}$$

Now that we have a small signal model for the MOSFET we can analyze amplifier circuits with small signal analysis using the following procedure:

1. Use DC analysis to find the operating point. In particular we must find either V_{GS} or I_D to determine g_m.
2. Insert the MOSFET small signal model into the small signal equivalent circuit.
3. Analyze the small signal circuit to find gain or other small signal parameters of interest.

As we did with diodes, we construct the small signal equivalent circuit by replacing independent voltage sources with short circuits and the independent current sources are replaced with open circuits. Independent voltage sources are replaced with short circuits because a change in current through the voltage source results in no change in voltage because the voltage produced by an ideal voltage source is completely independent of the current produced by the source.

$$\Delta v_{voltage\ source} = 0 \times \Delta i_{voltage\ source}$$

$$\therefore r_{voltage\ source} = 0$$

In other words the small signal resistance of the voltage source is zero because small changes in current produce no change in voltage (i.e. $r_{\text{voltage source}} = dv/di = 0$).

Similarly, an ideal current source is replaced with an open circuit because the current produced by an independent current source is not affected by changes in voltage across it.

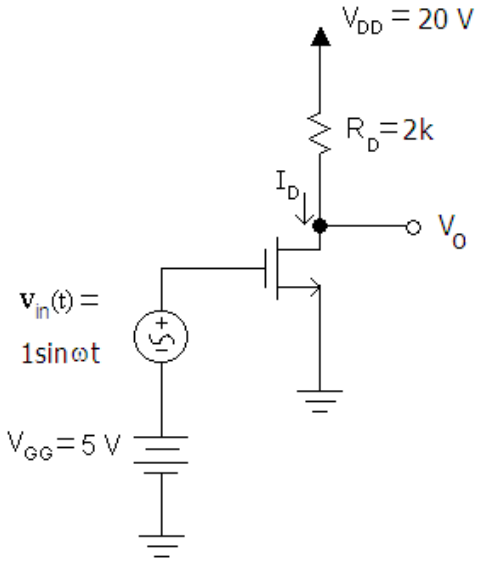
$$\Delta i_{current\ source} = 0 \times \Delta v_{current\ source}$$

$$\therefore r_{current\ source} = \infty$$

The current produced by an ideal current source is independent of changes in voltage ($r_{\text{current source}} = dv/di = \infty$).

Example 13: Using the Small Signal Model

Determine the small signal voltage gain (v_o/v_{in}) for the circuit below. Assume V_{Th}=1 V, K_n=0.25 mA/V^2.



In order to find the small signal model, we will find the drain current I_{DQ}. Finding I_{DQ} will also allow us to verify that the MOSFET is operating in the saturation region.

$$I_{DQ} = K_n(V_{GS} - V_{Th})^2$$

$$I_{DQ} = 0.25(5-1)^2 = 4\ mA$$

Using KVL to calculate the quiescent drain voltage yields:

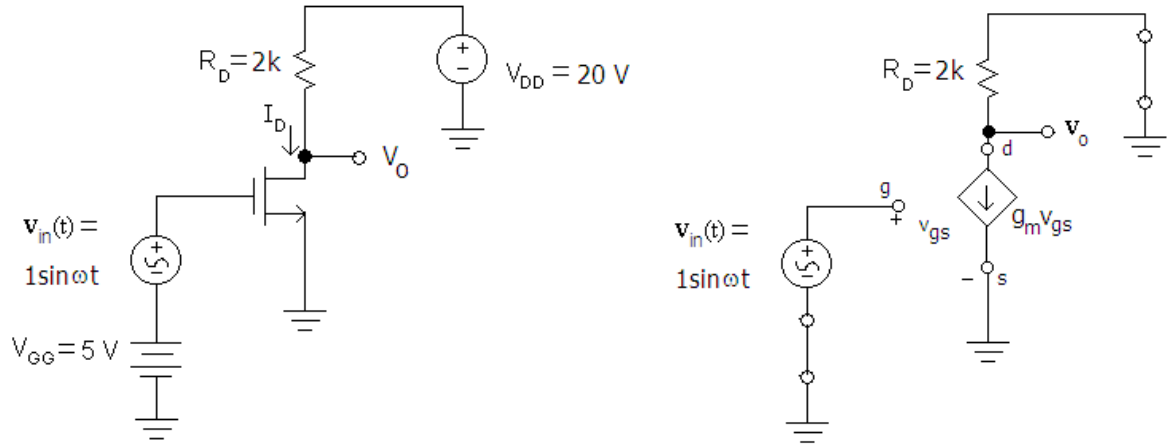
$$V_{DSQ} = 20 - 2k \times 4m = 12\ V$$

Therefore, the MOSFET is indeed operating in the saturation region ($V_{DS} \geq V_{GS}-V_{Th}$). The small signal parameter g_m can be found using:

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$g_m = 2\sqrt{0.25m \times 4m} = 2\ mS$$

We now construct the small signal model. Note that the DC voltage sources (V_{GG} and V_{DD}) have been replaced with short circuits (to ground):



Original Circuit Redrawn Showing V_{DD} | Small Signal Equivalent Circuit

Figure 64: Construction of Small Signal Equivalent Circuit

The small signal circuit shown above in Figure 64 can be further simplified to the circuit shown in Figure 65.

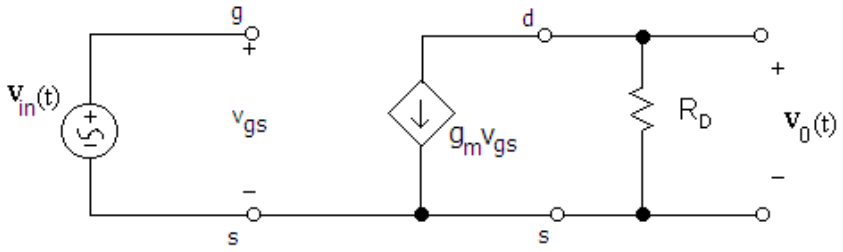


Figure 65: Simplified Small Signal Equivalent

To find the gain, we note that $v_{in} = v_{gs}$ and $v_o = -g_m v_{gs} R_D$. The negative symbol derives from the fact that the passive sign convention is not followed.

$$A_V = \frac{v_o}{v_{in}} = \frac{-g_m v_{gs} R_D}{v_{gs}} = -g_m R_D$$

Substituting values for the parameters in the voltage gain equation above yields:

$$A_V = -(2m)(2k) = -4\ V/V$$

The amplifier inverts the input signal and quadruples its voltage amplitude.

Simulation: Small Signal Model of Simple Amplifier

Practical Amplifier Circuits

In our previous analysis we analyzed a conceptual amplifier using small signal analysis to understand how MOSFETs can be used to amplify signals. We will now examine circuit configurations that are used in practical amplifier circuits. A popular bias circuit configuration used with discreet MOSFET amplifiers is the "four resistor bias network" shown in Figure 66. Note that this bias network requires only one power supply, V_{DD}. The R_1-R_2 voltage divider supplies the DC gate voltage required to bias the MOSFET in the saturation region.

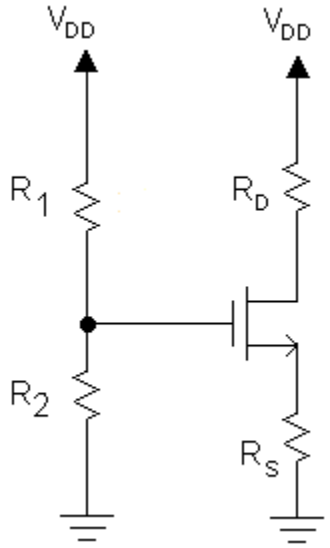


Figure 66: Four Resistor Bias Circuit

For the transistor to function as an amplifier we need some way to couple the input signal to the transistor. In the conceptual amplifier, the voltage at the gate consisted of a DC voltage source in series with an AC voltage source. For the four resistor bias network, a coupling capacitor can be used to couple the AC voltage source to the gate. In order to understand how this coupling works, we first introduce the concept of impedance.

Impedance is analogous to resistance in AC circuits and is equal to the AC voltage divided by the AC current. The magnitude of the impedance of a capacitor to AC signals is given by:

$$Z_C = \frac{1}{\omega C}$$

where C is the capacitance and ω is the radian frequency of the signal. Note that the impedance of a capacitor to DC signals (ω=0) is infinite and for high frequency AC signals the impedance is quite small. This is an important result that we will use as we construct AC (small signal) and DC models of transistor circuits that contain capacitors. We will assume that the values of frequency and capacitance are sufficiently large that we can approximate using an open circuit for DC and a short circuit for high frequency AC signals as shown in Figure 67.

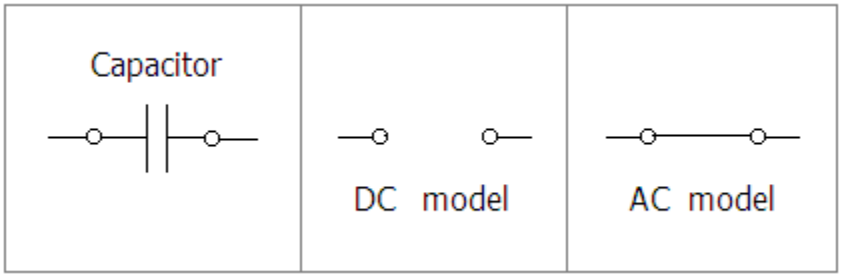


Figure 67: DC and AC Capacitor Models

We shall apply these models to the left side of the four resistor bias network shown in Figure 68. To find the total voltage v_G we find the DC and AC components and add them together.

$$v_G = V_G + v_g$$

$$\underbrace{v_G}_{\text{total}} = \underbrace{V_{DD} \times \left(\frac{R_2}{R_1 + R_2}\right)}_{\text{DC}} + \underbrace{v_{in}}_{\text{Small signal}}$$

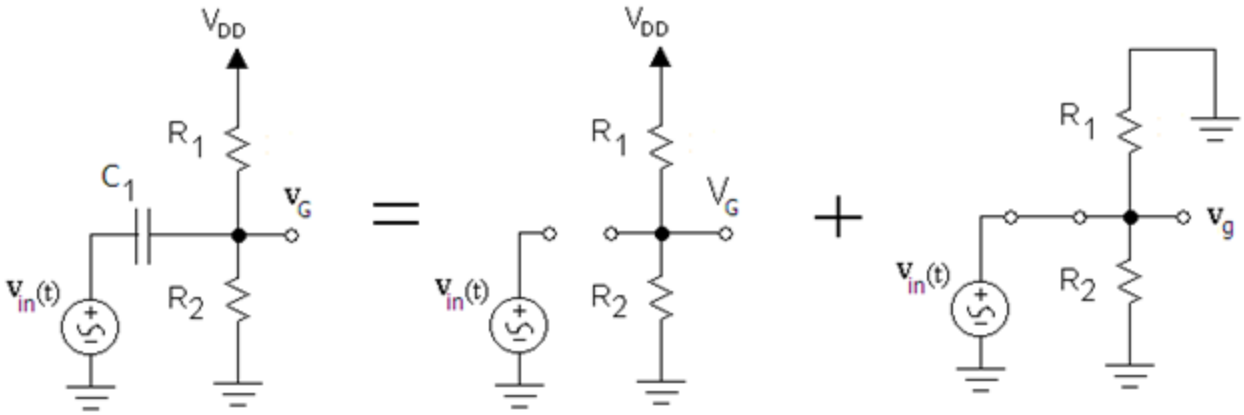


Figure 68: Capacitor AC and DC models

Note that for the AC model we have replaced the capacitor with a short circuit and the DC voltage source with a short circuit to ground. The voltage at the gate is equal to the DC voltage plus the AC voltage.

Simulation: Capacitive Coupling

Common Source Amplifier

The circuit shown in Figure 69 uses capacitive coupling and the four resistor bias network and is known as a Common Source (CS) amplifier configuration. The term "common source" is used because the source terminal is connected to AC ground as we shall see shortly.

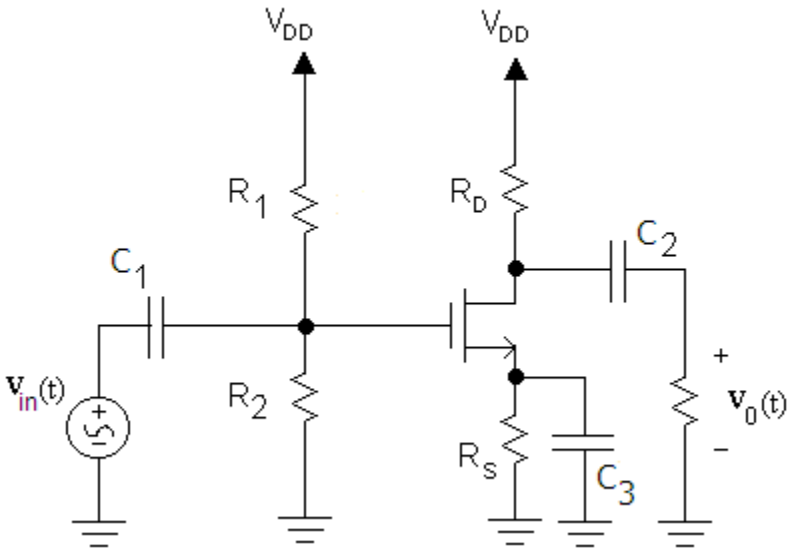


Figure 69: Common Source Amplifier

To analyze this amplifier using small signal analysis we start by redrawing the circuit where the voltage sources V_{DD} are inserted as shown in Figure 70.

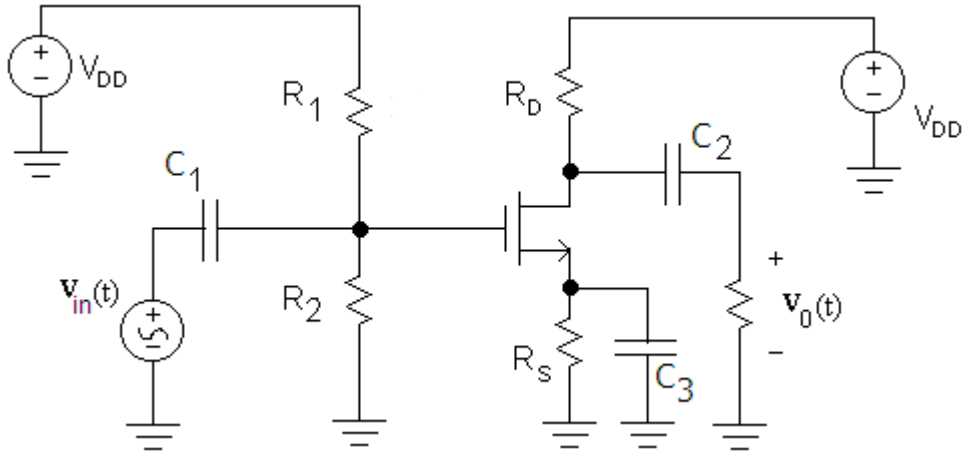


Figure 70: Common Source Amplifier with Voltage Sources Drawn

To draw the small signal equivalent circuit we note the following:

- Capacitors are assumed to be short circuits to the small signals.
- Voltage sources are assumed to be short circuits to the small signals.
- Current sources are assumed to be open circuits to the small signals.

The small signal equivalent circuit is shown in Figure 71.

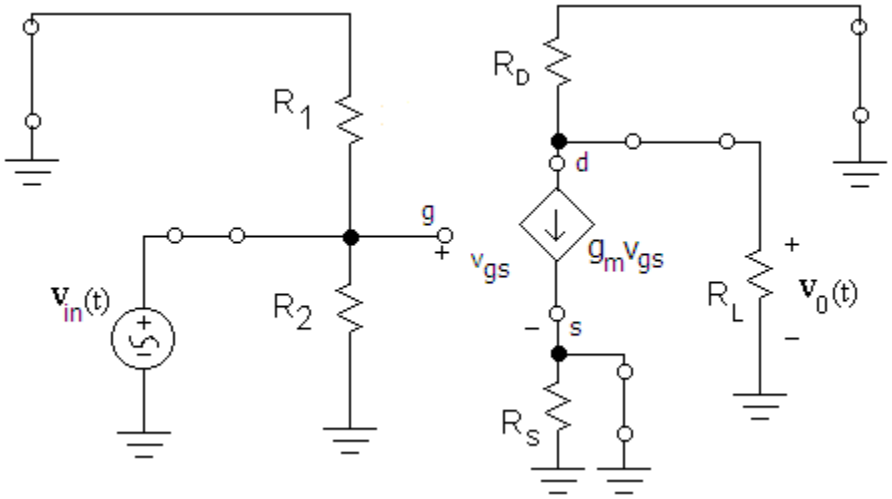


Figure 71: Small Signal Equivalent of Common Source Amplifier

We will redraw the circuit to make it clearer as shown in Figure 72.

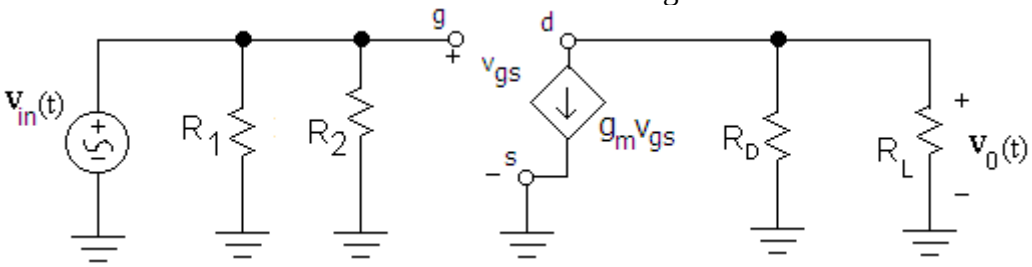


Figure 72: Simplified Small Signal Equivalent of Common Source Amplifier

Note that resistor R_3 has been eliminated because the capacitor C_3 provides a bypass to ground in the small signal equivalent circuit.

To calculate the small signal voltage gain we find that:

$$v_{gs} = v_{in}$$

$$v_o = -g_m v_{gs}(R_D // R_L)$$

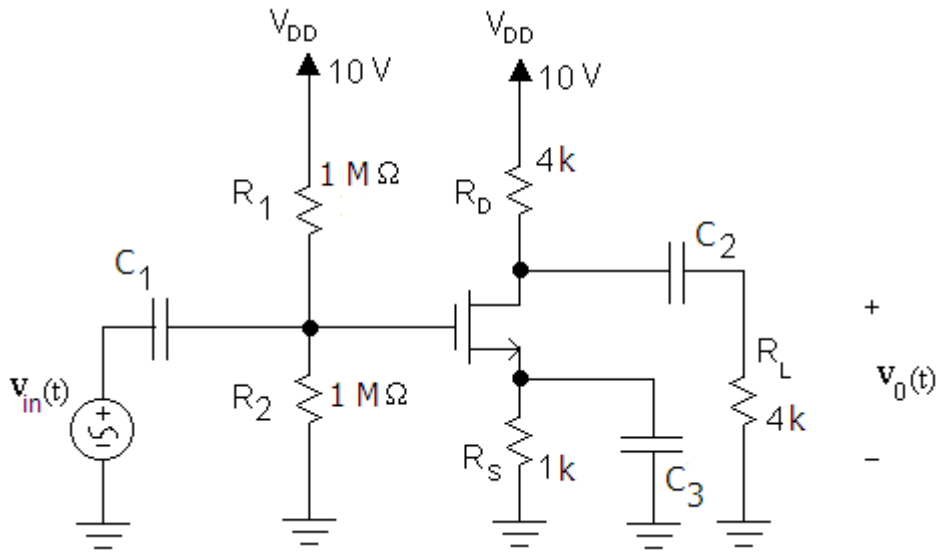
$$A_V = \frac{v_o}{v_{in}} = \frac{-g_m v_{gs}(R_D // R_L)}{v_{gs}} = -g_m(R_D // R_L)$$

Where $g_m = 2\sqrt{K_n I_{DQ}}$

Simulation: Common Source Amplifier

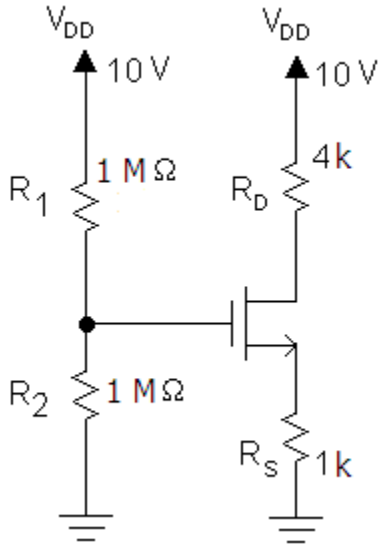
Example 14: Common Source Amplifier.

Find the voltage gain A_V of the following circuit. Assume V_{Th}=2 V, K_n=0.25 mA/V^2.



In order to find the small signal parameter g_m, we must find the quiescent current I_{DQ}. We draw the DC equivalent of the circuit and note that the capacitors are assumed to be sufficiently large to be considered open circuits to DC.

We obtain the DC model below.



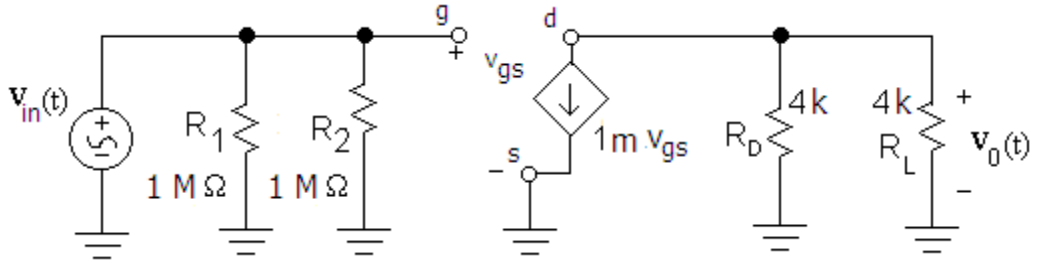
This circuit has been analyzed in a previous example where we obtained I_D=1 mA. This is the quiescent current I_{DQ} for our amplifier. We now calculate the small signal transconductance as follows:

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$g_m = 2\sqrt{(0.25m)(1m)}$$

$$g_m = 1\,mS$$

Next, we construct the small signal equivalent circuit as shown below.

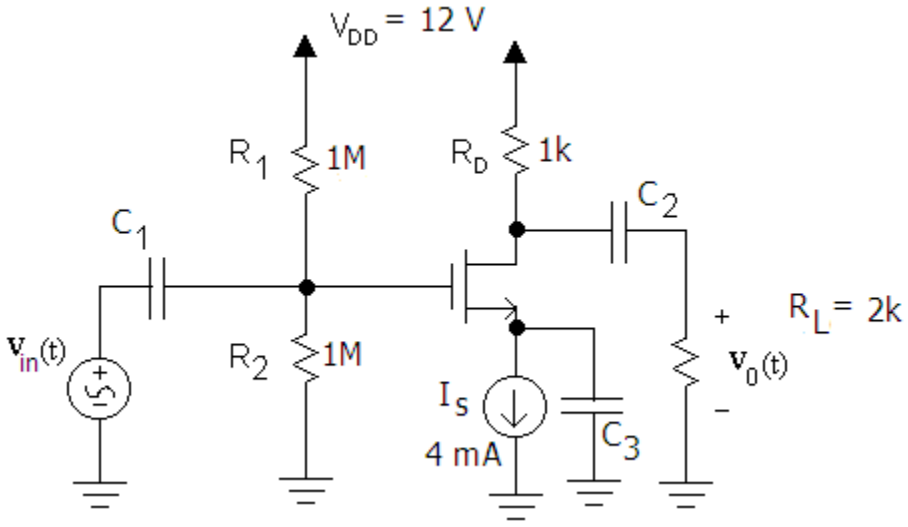


This is the same circuit as the one in Figure 72. Using the formula derived earlier:

$$A_V = -g_m(R_D//R_L)$$
$$A_V = -1m(4k//4k)$$
$$A_V = -2\ V/V$$

Example 15: Common Source Amplifier Biased with a Current Source

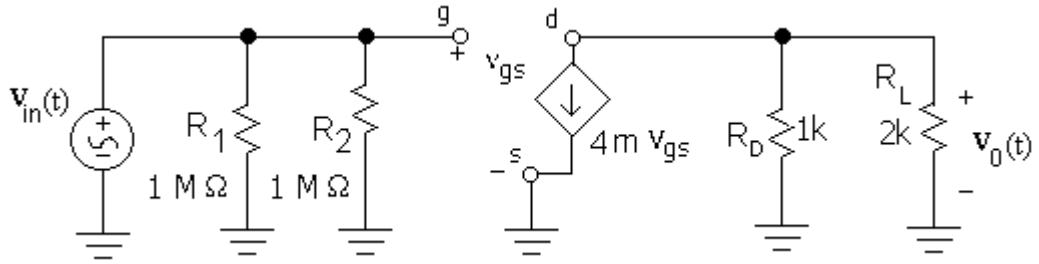
Find the voltage gain A_V for the circuit below. Assume that K_n=1 mA/V^2 and V_{Th}=1 V.



The large signal equivalent is the same as the bias circuit example analyzed previously and we found the circuit operated in the saturation region with I_D=4 mA. We now calculate the small signal transconductance as follows:

$$g_m = 2\sqrt{K_n I_{DQ}}$$
$$g_m = 2\sqrt{(1m)(4m)}$$
$$g_m = 4\ mS$$

Next, we construct the small signal equivalent circuit as shown below. The current source is replaced with an open circuit, the voltage sources with short circuits, and the coupling and bypass capacitors are replaced with short circuits. The result is shown below.



$$A_V = \frac{v_o}{v_{in}} = \frac{-g_m v_{gs} R_D // R_L}{v_{gs}} = -g_m R_D // R_L$$

$$A_V = -4m \times (1k // 2k) = -2.67\ V/V$$

Source Follower Amplifier

The source follower amplifier is used as a power amplifier. As we will discover, the voltage gain is less than one but the amplifier does provide a current gain that is greater than 1. It has a high input resistance and a low output resistance which makes it ideal as a buffer to reduce loading effects. For instance, the gain of the common source amplifier by the load attached to it. If a buffer is placed between the output of the CS amplifier and the load, the CS amplifier's gain will be independent of the load since the buffer's high input impedance acts as a large load resistance (ideally infinite). A source follower amplifier is shown in Figure 73 below.

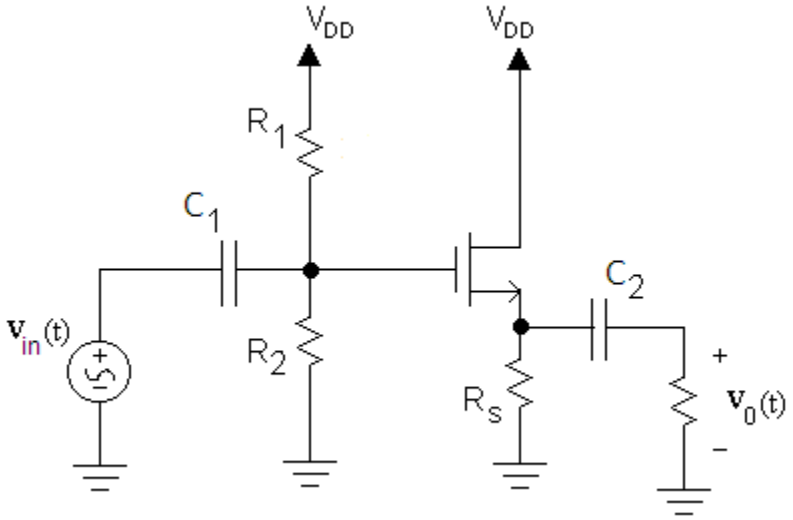


Figure 73: Source Follower Amplifier

As was the case with the common source amplifier, the capacitors C_1 and C_2 are used to couple the input and output to the amplifier bias circuit. Next, we construct the small signal equivalent.

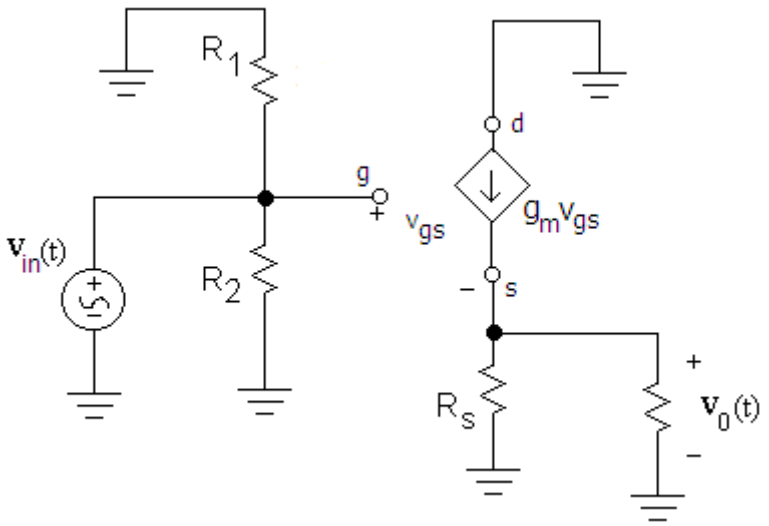


Figure 74: Small Signal Equivalent of Source Follower

We will redraw this circuit to make it easier to analyze.

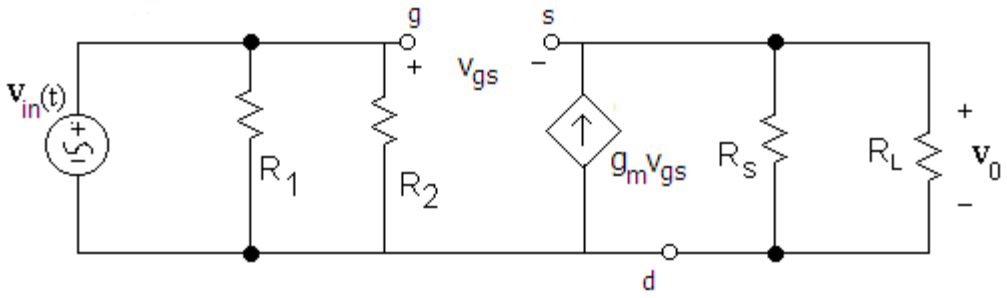


Figure 75: Small Signal Equivalent of Source Follower Simplified

The output voltage is:

$$v_o = v_s = g_m v_{gs}(R_s // R_L)$$

The voltage v_{gs} can be found as follows:

$$v_g = v_{in}$$

$$v_{gs} = v_g - v_s$$

$$v_{gs} = v_{in} - g_m v_{gs}(R_s // R_L)$$

$$v_{gs} = \frac{v_{in}}{1 + g_m(R_s // R_L)}$$

Substituting into the v_o equation above:

$$v_o = g_m \left[\frac{v_{in}}{1 + g_m(R_s // R_L)}\right](R_s // R_L)$$

$$A_v = \frac{g_m(R_s//R_L)}{1 + g_m(R_s//R_L)}$$

The denominator must be greater than the numerator so the voltage gain must be less than 1. The source follower amplifier does not produce a larger output than the input voltage. Next we analyze the current gain to show that it functions well as a buffering amplifier.

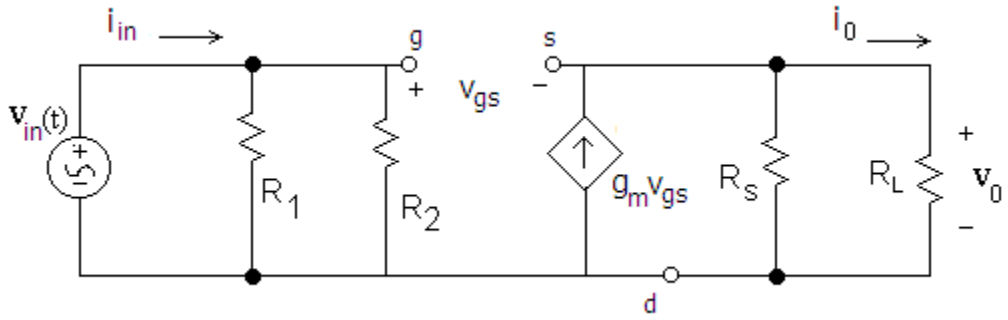


Figure 76: Current Gain for Source Follower

From the derivation of A_V we found:

$$v_o = g_m\left[\frac{v_{in}}{1 + g_m(R_s//R_L)}\right](R_s//R_L)$$

We can write v_o and v_{in} in terms of i_o and i_{in} as follows:

$$v_0 = i_o R_L$$

$$v_{in} = i_{in} \times (R_1//R_2)$$

Substituting these into the one above yields:

$$i_o R_L = g_m\left[\frac{i_{in}(R_1//R_2)}{1 + g_m(R_s//R_L)}\right](R_s//R_L)$$

$$A_i = \frac{i_o}{i_{in}} = \frac{g_m}{R_L}\left[\frac{(R_1//R_2)}{1 + g_m(R_s//R_L)}\right](R_s//R_L)$$

$$A_i = \frac{(R_1//R_2)}{R_L}\left[\frac{g_m(R_s//R_L)}{1 + g_m(R_s//R_L)}\right]$$

$$A_i = \frac{(R_1//R_2)}{R_L}[A_V]$$

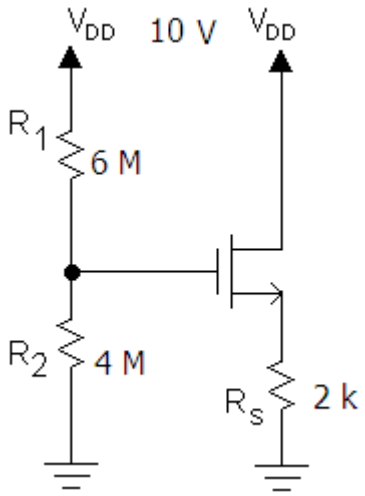
Assuming that A_V is close to 1, the current gain can be substantial if we make R_1 and R_2 large in comparison to R_L.

Simulation: Source Follower Amplifier

Example 16: Source Follower Amplifier

Find the current gain and the voltage gain for a source follower amplifier shown in Figure 73 that has the following parameters: V_{DD}=10 V, R_1=6 MΩ, R_2=4 MΩ, K_n=2 mA/V^2, R_S=2 kΩ, R_L=3 kΩ and V_{Th}=1 V.

In order to find the transconductance parameter g_m, we must find the quiescent train current I_{DQ}. The DC transistor model is shown below.



Using voltage division, we calculate V_G= 4 V. Using Ohm's law, we find V_S=2kI_D. Therefore:

$$V_{GS} = 4 - 2kI_D$$

Substituting this equation into the MOSFET saturation current equation yields:

$$I_D = K_n(V_{GS} - V_{Th})^2$$

$$I_D = 2m\left((4 - 2kI_D) - 1\right)^2$$

$$I_D = \cancel{2\ mA}\ and\ 1.125\ mA$$

We now calculate g_m:

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$g_m = 2\sqrt{(2m)(1.125m)}$$

$$g_m = 3.00\ mS$$

The voltage gain and current gain can be calculated from the equations derived previously for the source follower amplifier.

$$A_v = \frac{g_m(R_s//R_L)}{1 + g_m(R_s//R_L)}$$

$$A_v = \frac{3.0m(2k//3k)}{1 + 3.0m(2k//3k)} = 0.783\ {}^{V}/_{V}$$

$$A_i = \frac{(R_1//R_2)}{R_L}[A_V]$$

$$A_i = \frac{(6M//4M)}{3k}[0.783] = 626\ {}^{A}/_{A}$$

This amplifier has an output current that is 626 times larger than the input current.

Voltage Amplifier Model

An ideal amplifier would take the input voltage and produce an output voltage that is a scaled replica of the input voltage that would be independent of the circuit connected to the input and the load connected to the output. However, the gain of real amplifiers is affected by these factors. We can model these effects using the voltage amplifier model below.

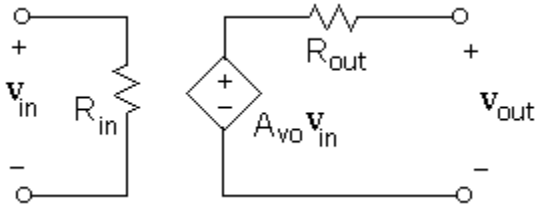


Figure 77: Voltage Amplifier Model

$$A_{vo} = \left.\frac{v_o}{v_{in}}\right|_{R_L=\infty}$$

The resistance R_{in} accounts for the fact that real amplifiers typically draw some current from the signal source. R_{out} is used to account for the fact that as increasing current flows from the amplifier's output terminals, the output voltage is reduced. A_{VO} is called the open circuit voltage gain; this is the gain if there is no load across the output terminals.

For instance, if we attach a practical voltage source (an ideal voltage source in series with its internal resistance) to the amplifier input and a load at its output, we can clearly see the impact of R_{IN} and R_{OUT} on voltage gain. If R_{in} were infinite, then $v_{in}=v_s$. Because R_{IN} is finite, v_{in} will be smaller than v_s. The actual voltage gain of the amplifier (v_{out}/v_s) will be reduced. On the output side we see that R_{OUT} and R_{LOAD} form a voltage divider and therefore the load voltage will be reduced as R_{OUT} becomes smaller. An ideal voltage amplifier has Rin = ∞ and R_{OUT} =0 because under these conditions the gain of the amplifier is completely independent of R_S and R_{LOAD}. If R_{OUT} were zero, then $V_{out} = A_{VO}V_{in}$.

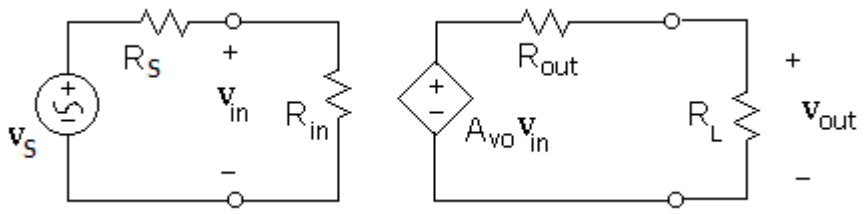


Figure 78: Voltage Amplifier Model Terminated with Source and Load

Calculating R_{in} and R_{out}

We apply these ideas by calculating the R_{in} and R_{out} of a common source amplifier. The small signal model for the amplifier is shown in Figure 79.

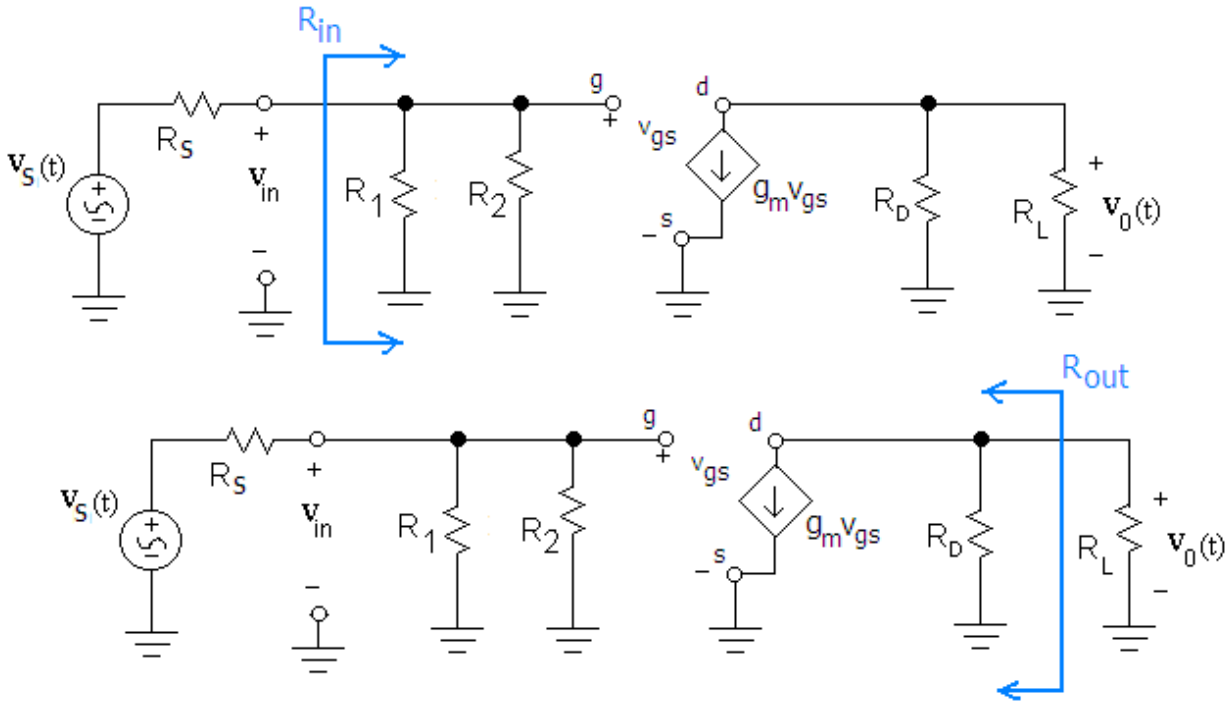


Figure 79: Small Signal Input and Output Resistances

R_{in} is the resistance seen looking into the input terminals of the amplifier. In this case, we can tell by inspection that this resistance is $R_1//R_2$. Note that for this particular amplifier, R_{in} is independent of R_L (this is not always the case!).

R_{out} is the resistance at the output of the amplifier which is the Thevenin resistance from the vantage point of R_L. To find R_{out}, we set signal sources to zero and apply a test voltage and determine the resulting test current. The output resistance is:

$$R_{out} = \frac{v_{test}}{i_{test}}$$

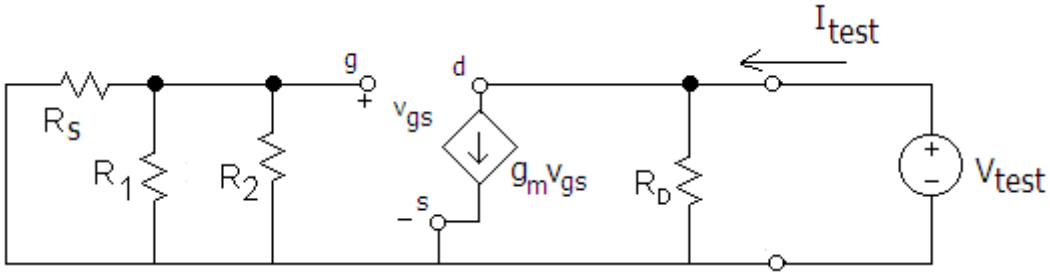


Figure 80: Circuit to Determine Rout

Using KCL at the top right node yields:

$$g_m v_{gs} + \frac{V_{test}}{R_D} - I_{test} = 0$$

We see that v_{gs}=0. Therefore:

$$I_{test} = \frac{V_{test}}{R_D}$$

Which yields:

$$R_{out} = \frac{V_{test}}{I_{test}} = \frac{V_{test}}{\frac{V_{test}}{R_D}} = R_D$$

We could shorten the analysis by simply noting that the dependent current source can be replaced by an open circuit because v_{gs}=0 and tell by inspection that R_{out}=R_D. It is important to note that R_{out} is independent of R_S, this is not always the case.

Next we calculate A_{VO}, the open voltage gain.

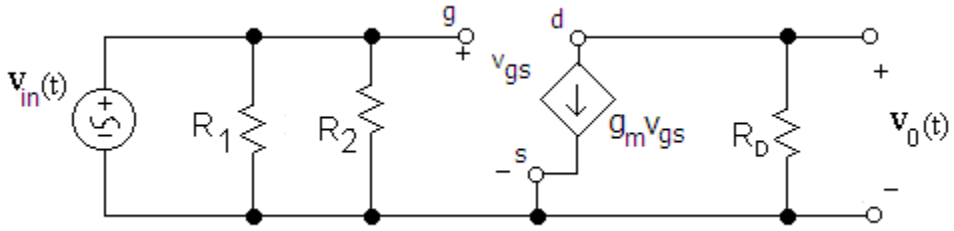


Figure 81: Finding A_{VO} for a Common Source Amplifier

By inspection we see that v_o=- $g_m v_{gs} R_D$. We note that v_{gs}=v_{in} so the open circuit gain is:

$$A_{vo} = \frac{v_o}{v_{in}}\bigg|_{R_L=\infty} = -g_m R_D$$

Now that R_{in}, R_{out}, and A_{VO} have been determined, we can construct the voltage amplifier model for the common source amplifier as shown in Figure 82.

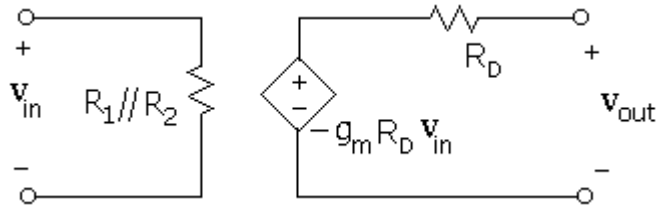


Figure 82: Voltage Amplifier Model of a Common Source Amplifier

We can use this model to determine the voltage gain (or other parameters of interest) of a common source amplifier that has a load and/or practical source attached to it. To illustrate this idea, we will attach the same load and source that was used in our initial examination of the common source amplifier. This circuit is shown in Figure 83 below.

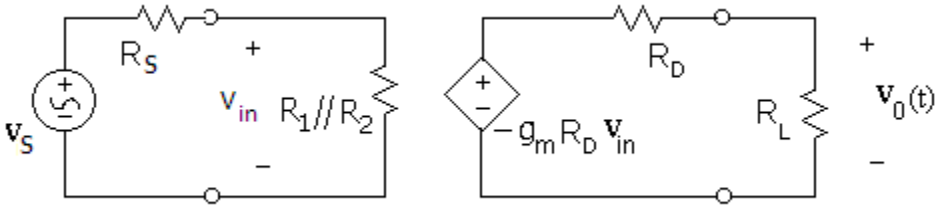


Figure 83: Voltage Amplifier Model with Source and Load Attached

We can calculate the output voltage v_o using voltage division:

$$v_o = -g_m R_D v_{in}\left(\frac{R_L}{R_D + R_L}\right)$$

For v_{in} we can write:

$$v_{in} = v_s\left(\frac{R_1 // R_2}{R_1 // R_2 + R_S}\right)$$

Therefore, the gain is:

$$A_v = \frac{v_o}{v_s} = -g_m R_D\left(\frac{R_L}{R_D + R_L}\right)\left(\frac{R_1 // R_2 + R_S}{R_1 // R_2}\right)$$

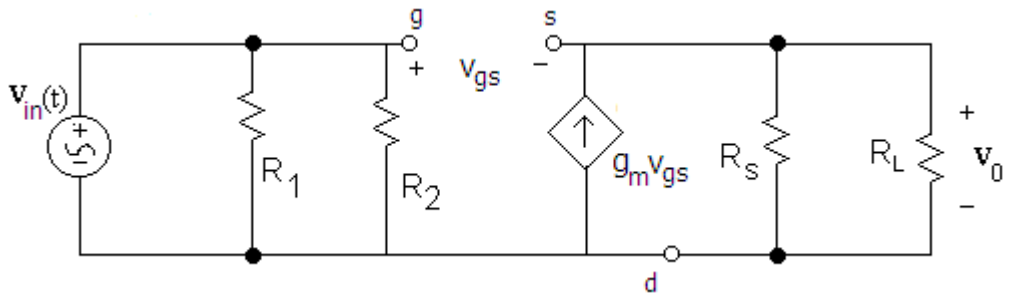
If we set R_S=0 then the equation above reduces to:

$$A_V = \frac{v_o}{v_s} = -g_m R_D\left(\frac{R_L}{R_D + R_L}\right) = -g_m\left(\frac{R_D R_L}{R_D + R_L}\right) = -g_m R_D // R_L$$

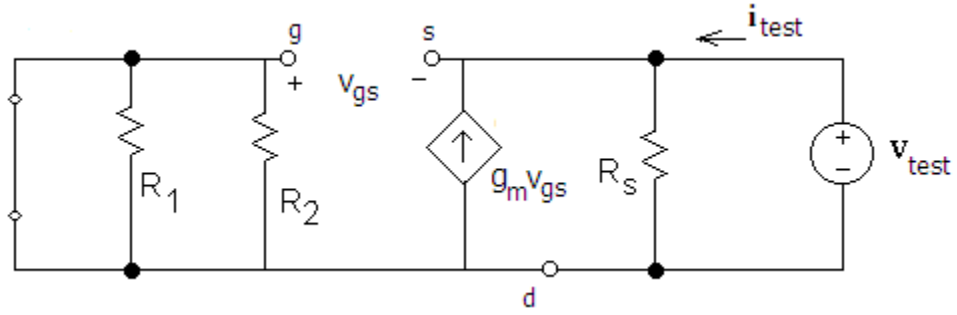
This is the same result that we derived previously. The value of the voltage amplifier model is that it gives us a sense of how output and input resistances affect the overall gain of our amplifier. Ideally, we would like to have an amplifier that has a high input resistance and a low output resistance.

Example 17: Voltage Amplifier Model of a Source Follower

Determine the voltage amplifier model of the source follower amplifier below.



This is the small signal model of the source model amplifier analyzed previously. By inspection, the input resistance $R_{in}=R_1//R_2$. The circuit to determine the output resistance is shown below.



The gate voltage $v_g=0$. The voltage at the source $v_s=v_{test}$. Therefore $v_{gs}= -v_{test}$. Applying KCL at the top right note yields:

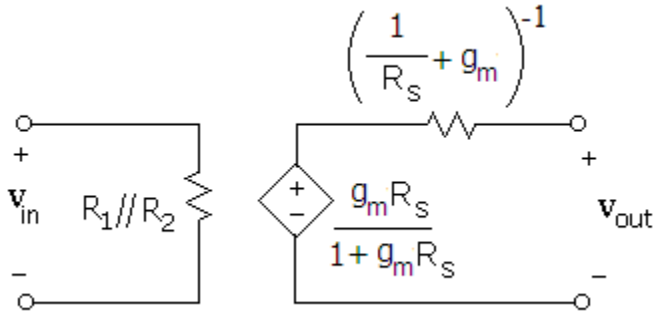
$$i_{test} = \frac{v_{test}}{R_S} - g_m \times (-v_{test})$$

$$R_{out} = \frac{v_{test}}{i_{test}} = \left(\frac{1}{R_S} + g_m\right)^{-1}$$

Finally, we calculate A_{VO}. We can use the equation derived previously but set $R_L = \infty$.

$$A_{vo} = \frac{g_m(R_s//\infty)}{1 + g_m(R_s//\infty)} = \frac{g_m R_s}{1 + g_m R_s}$$

The complete model for the source follower is shown below.



Small Signal Drain Resistance Parameter r_D

The small signal model for the MOSFET that we have been using assumes that the drain current i_D is independent of v_{DS}. However, in reality i_D increases as v_{DS} increases as shown in Figure 84.

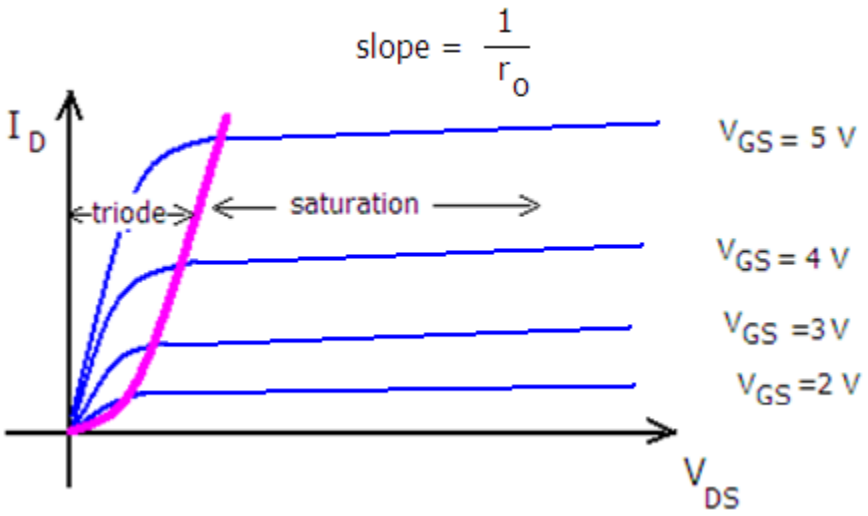


Figure 84: Effect of V_{DS} on I_D in Saturation

Note the slope of the line is not horizontal as we had assumed previously. To account for this in the saturation equation, we introduce the device parameter λ and modify the saturation equation as shown below:

$$\boldsymbol{CURRENT}: \quad i_D = K_n(v_{GS} - V_{Th})^2 \times (1 + \lambda v_{DS})$$

Note that if λ=0, the equation reduces to the saturation equation that we have used thus far. For the small signal model, the i_D dependency on v_{DS} can be accounted for by adding a large resistor called the drain resistance r_d in parallel with the transconductance as shown in Figure 85. The resistor causes the small signal drain current i_d to increase as v_{ds} increases. The value of r_d is the inverse slope of the characteristic line for a particular v_{GS}. More formally:

$$r_d = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}\Bigg|_{for\ constant\ v_{GS}}$$

$$r_d = [\lambda \times K_n(v_{GS} - V_{Th})^2]^{-1}$$

$$r_d = [\lambda I_{DQ}]^{-1}$$

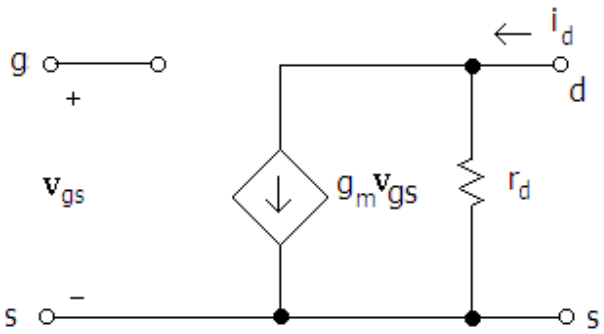
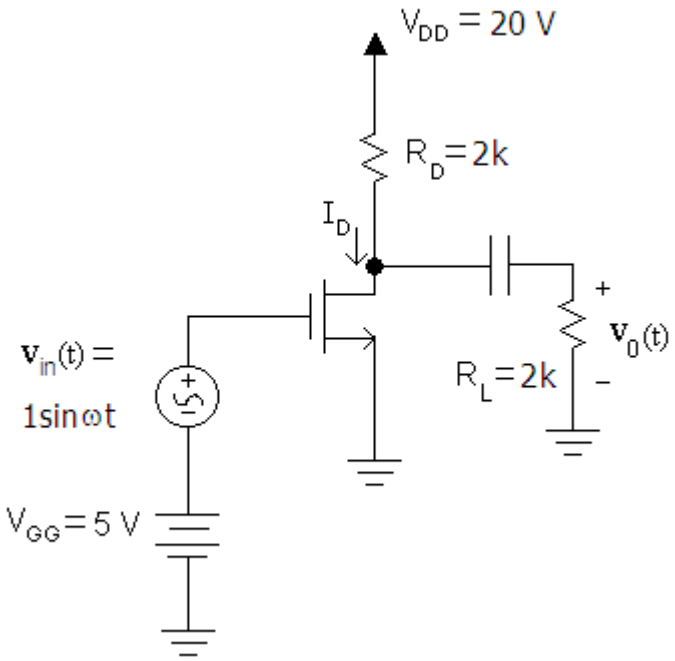


Figure 85: Small Signal Model Including r_d.

If the slope of the characteristic line is horizontal, the value of r_d is infinite, and the model reduces to the model that we have used previously.

Example 18: Effect of λ on Small Signal Model

Determine the small signal model of the amplifier below. Assume that K_n=0.25 mA/V^2, V_{Th}=1 V, and λ= 0.01 V^{-1}.



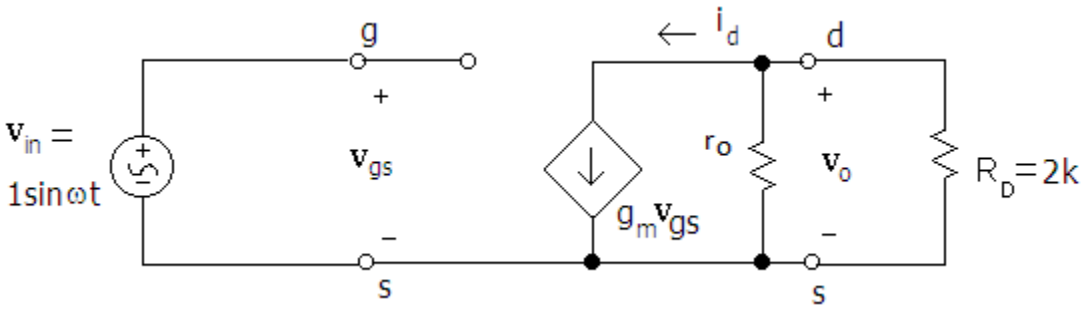
To determine the small signal model parameters g_m and r_o we must first determine I_{DQ}. From our previous analysis (see Example 13) we determined I_{DQ}= 4 mA. Therefore

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$g_m = 2\sqrt{0.25m \times 4m} = 1\ mS$$

$$r_o = [\lambda I_{DQ}]^{-1}$$
$$r_o = [0.01 \times 4\text{m}]^{-1}$$
$$r_o = 25\ k\Omega$$

We now construct the small signal model.



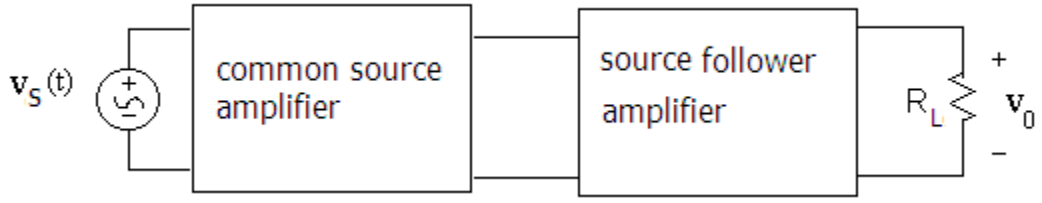
To find the gain, we note that $v_{gs} = v_{in}$ and $v_o = -g_m v_{gs}(R_D // r_o)$. Therefore

$$A_V = \frac{v_o}{v_{in}} = \frac{-g_m v_{gs}(R_D//r_0)}{v_{gs}} = -g_m(R_D//r_0)$$
$$A_V = -1(2k//25k)$$
$$A_V = -1.85\ V/V$$

The gain decreases when we include the output resistance.

Multistage Amplifiers

We have looked at two amplifier configurations: The Common Source amplifier and the Source Follower amplifier. By combining these amplifiers, we can construct an amplifier that combine the best features of both. In the multistage amplifier below, the common source amplifier provides the voltage gain while the source follower provides a low output resistance. The low output resistance will cause the gain to be relatively independent of R_L.



Amplifier Distortion and Clipping

An ideal amplifier will produce a scaled replica of the input voltage signal. In actuality, the signal will be distorted because the i_D vs. v_{GS} characteristic curve is nonlinear. The amplifier will

produce second order distortion as a result. Referring to the discussion on load line analysis we can see that the output voltage signal Q point is not midway between the upper and lower peaks.

Clipping occurs when the MOSFET is no longer operating in the saturation region. For instance, if the input voltage plus the bias voltage is less than V_{Th} the MOSFET will be in cutoff. The amplifier will also clip the input signal if the MOSFET enters the triode region. This can occur when the R_D is too high. Circuit designers must carefully bias the transistor so that the MOSFET remains in the saturation region.

Simulation: MOSFET Clipping

Summary

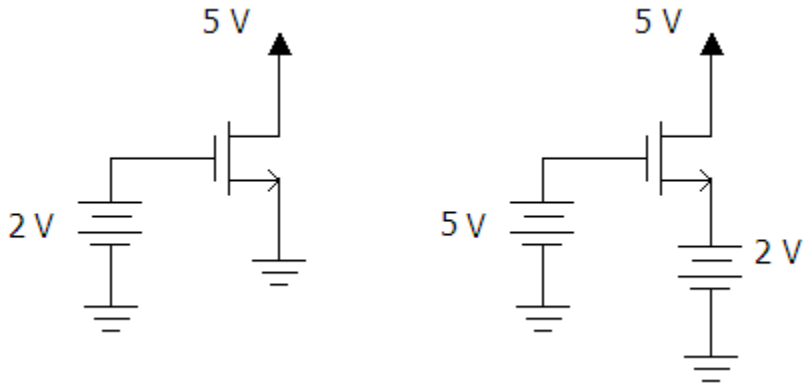
- The MOSFET is an extremely important device because it is found in many electronic devices.
- The MOSFET has 3 terminals: Gate, Drain, and Source. The voltage v_{GS} controls the drain current i_D.
- The MOSFET has 3 modes: cutoff, triode, and saturation.
- The triode mode is used in switching applications and to make voltage-controlled resistors
- The saturation mode is used for amplifiers.
- To perform MOSFET DC analysis, we assume an operating region, calculate the variables of interest, and check to make sure that the assumption was correct.
- MOSFETs can be used to perform logic functions.
- The small signal model of the MOSFET is used to approximate how it behaves to small changes in response to small changes in gate voltage.
- Two common amplifier configurations are the common source amplifier and the source follower.
- The common source amplifier can be used to provide voltage gain.
- A MOSFET small signal model can include a small signal drain resistance to account for the slight dependence of v_{DS} on i_D in saturation.
- The source follower amplifier can be used to provide current gain. It has a low output resistance compared to the common source amplifier.
- The voltage amplifier model can be used to simplify the analysis of amplifier circuits subjected to input signals with internal resistances and finite output load resistances.
- Amplifiers can be combined into multistage amplifiers for better performance.
- Amplifiers distort the input signal because the i_D vs. v_{GS} is non-linear.
- The output signal will be clipped if the MOSFET leaves the saturation region.

List of Examples

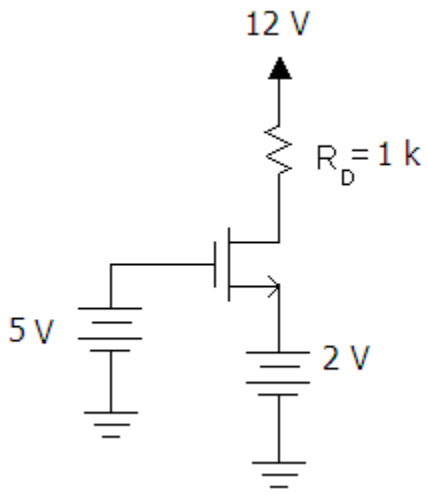
Table of Figures

Problems

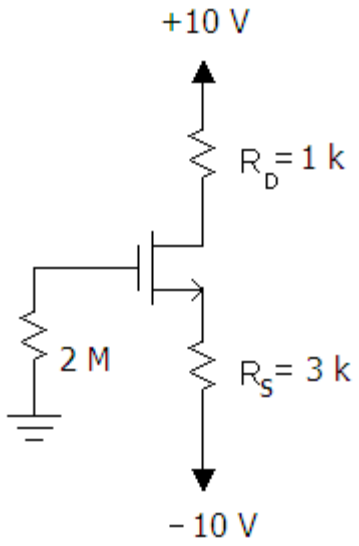
1. An NMOS transistor with K_n=1 mA/V^2 and V_{Th}=1 V is operated with V_{GS} = 2.5 V. At what value of V_{DS} does the transistor enter the saturation region? What value of I_D is obtained in saturation?
2. An NMOS transistor with parameters V_{Th}=1 V, k'=100 μA/V^2, W = 10 μm, and L=1 μm has a V_{DS}=1.5 V. Find the drain current when:
    a. V_{GS}=0.5 V
    b. V_{GS}=2 V
    c. V_{GS}=3 V
3. An NMOS transistor with parameters V_{Th}=1 V, k'=100 μA/V^2, W = 10 μm, and L=1 μm has a V_{GS}=2 V. Find the drain current when:
    a. V_{DS}=0.5 V
    b. V_{DS}=2 V
    c. V_{DS}=3 V
4. An NMOS transistor with parameters V_{Th}=1 V, k'=100 μA/V^2, and L=1 μm has a V_{DS}=0.5 V, V_{GS}=2 V, and I_D=1mA. Find the channel width W.
5. An NMOS transistor with parameters V_{Th}=1 V, k'=50 μA/V^2, L=2 μm and W=40 μm. Sketch I_D vs V_{DS} characteristic curves for V_{GS}=1, 2, 3, and 4 V for V_{DS} ranging from 0-10 V.
6. In the triode region, how does V_{GS} affect the drain to source resistance R_{DS}? Why does it have this effect?
7. Assume a MOSFET transistor operates in the triode region. How do the parameters L and W effect the drain to source resistance? Does this seem intuitive?
8. Determine the drain current for the circuits below. Assume that V_{Th}=1 V, k'=100 μA/V^2, W = 200 μm, and L=10 μm.



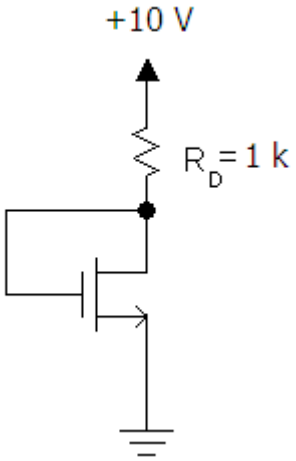
9. Find I_D and V_{DS} for the circuit shown below. The NMOS parameters are V_{Th}=1 V and K_n=0.25 mA/V^2.



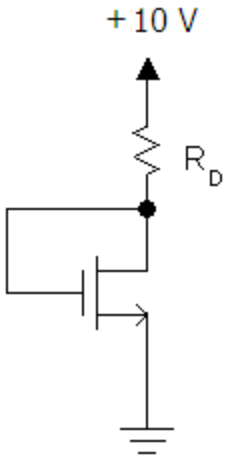
10. Find I_D and V_{DS} for the circuit shown below. The NMOS parameters are V_{Th}=1 V and K_n=0.25 mA/V^2.



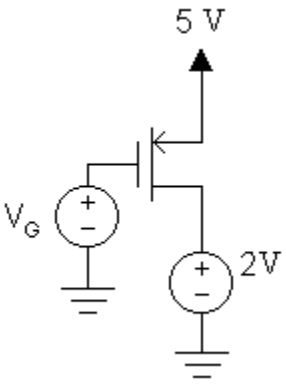
11. Find I_D and V_{DS} for the circuit shown below. The NMOS parameters are V_{Th}=1 V and K_n=0.25 mA/V^2.



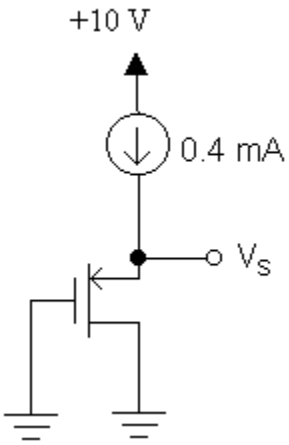
12. Design the circuit so that I_D=10 mA. The NMOS parameters are V_{Th}=1 V and K_n=0.25 mA/V^2.



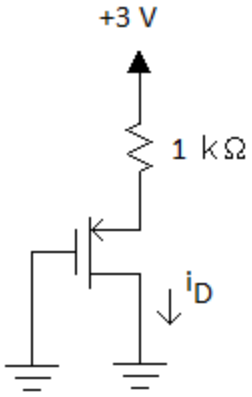
13. For the PMOS transistor below, assume that V_{Th}=-0.75 V. Determine the following:
    a. Maximum and minimum voltages for V_G so that the transistor is in saturation.
    b. What mode is the transistor in if V_G is above the maximum you found in part a?
    c. What mode is the transistor in if V_G is below the minimum you found in part a?



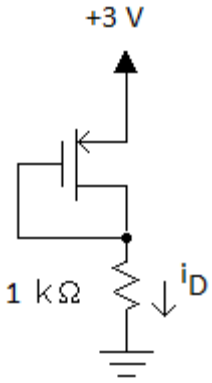
14. For the PMOS circuits below, find the desired parameter. Assume K_P=0.1 mA/V^2 and V_{Th}= -1V.
    a. Find the voltage V_S



    b. Find the current i_D.



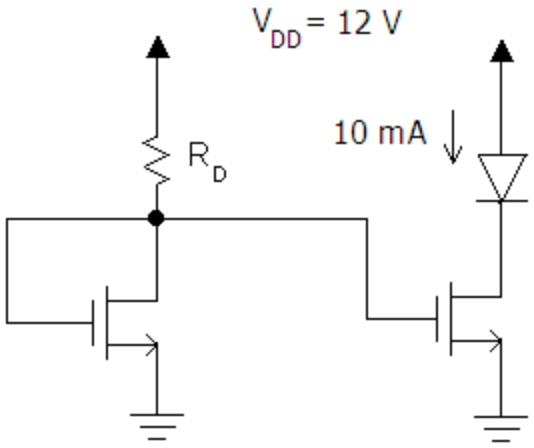
    c. Find the current i_D.

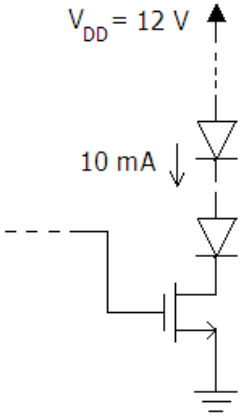


15. Design a circuit using MOSFETs that performs the logic NAND operation. The NAND operation is represented with the following truth table.

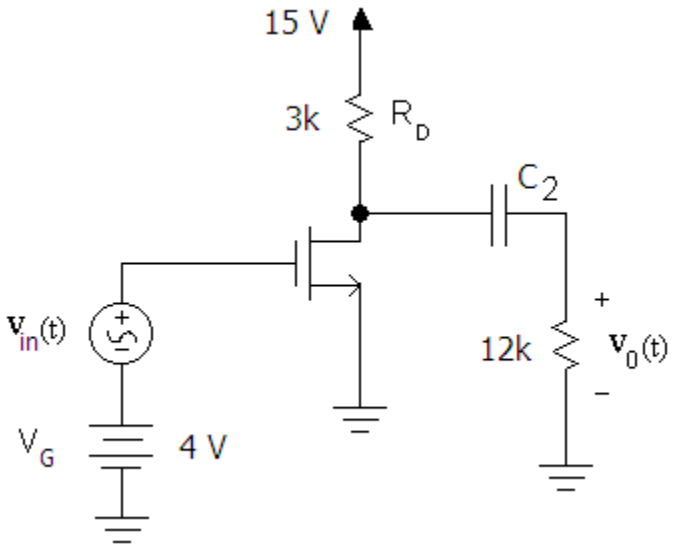
V_1	V_2	V_0
0	0	5 V
0	5 V	5 V
5 V	0	5 V
5 V	5 V	0

16. Design a current source using the current mirror configuration that produces a current of 10mA to illuminate an LED with a voltage drop of 2.1 V. How many such LEDs could be illuminated using your current source? Assume identical transistors each with K_n=1mA/V^2, V_{Th}=1V, and V_{DD}=12V.



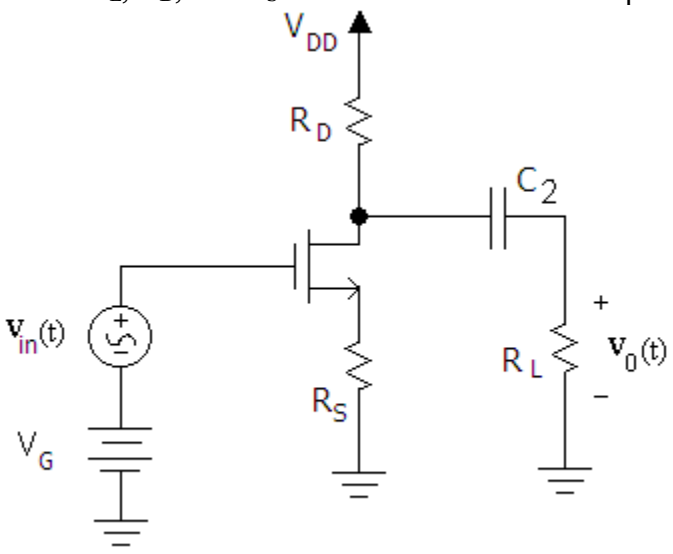


17. Determine the small signal voltage gain of the circuit below. Assume K_n=0.5 mA/V^2, and V_{Th}=2V.

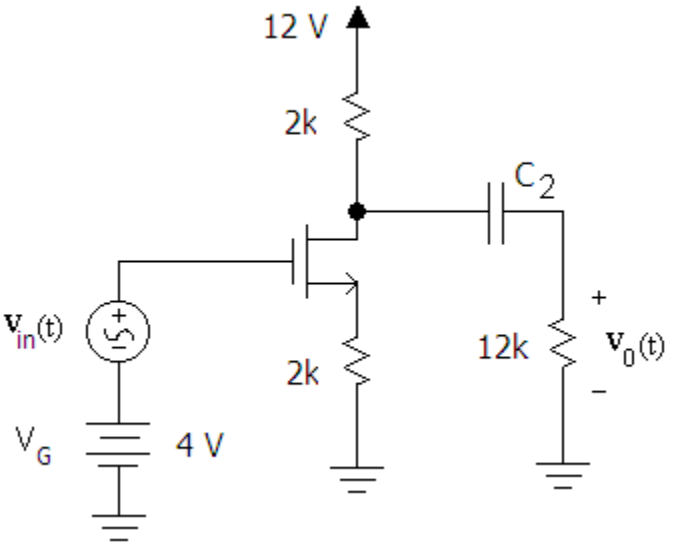


18. Determine the small signal output resistance of the circuit above. Assume K_n=1mA/V^2, and V_{Th}=1V.

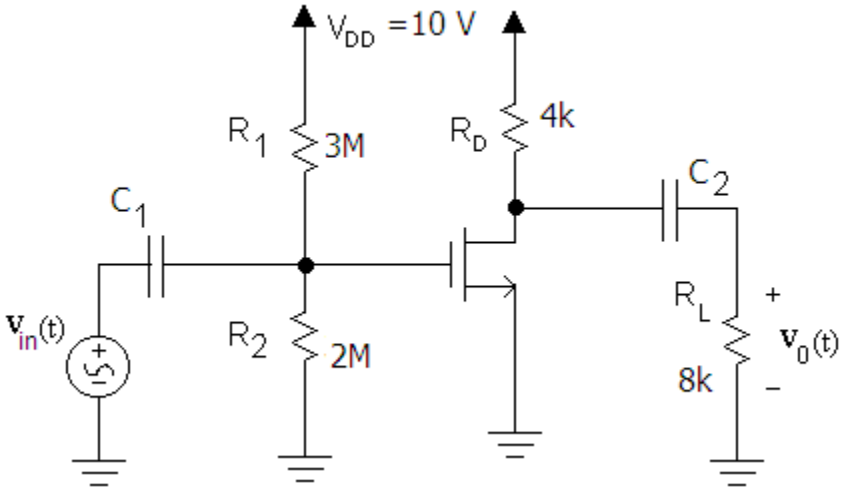
19. Derive the formula for the small signal voltage gain (A_V) in terms of g_m and the resistors R_L, R_D, and R_S. Assume the transistor is operating in the saturation region.



20. Determine the voltage gain of the circuit below. Assume K_n=1mA/V^2, and V_{Th}=1V.



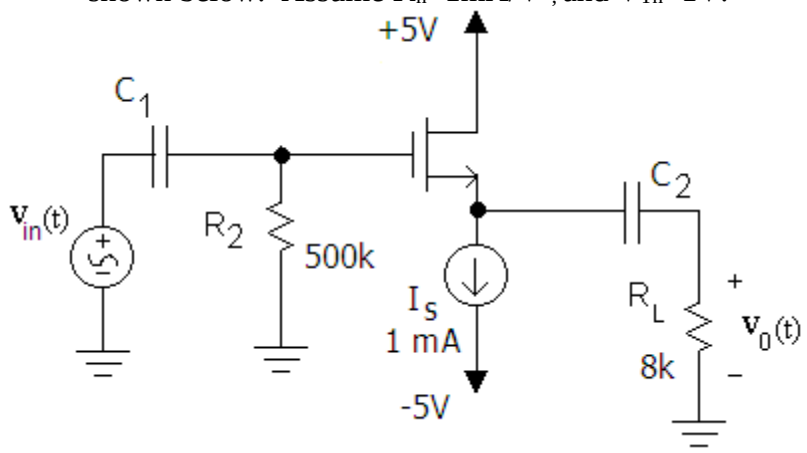
21. Determine the small signal voltage gain of the following circuit. Assume V_{Th}=2V and K_n=0.25 mA/V^2.



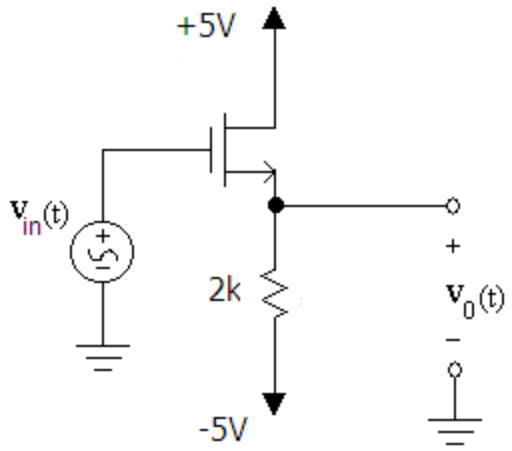
22. Determine the small signal R_{in} and R_{out} for the amplifier above.

23. Design a common source amplifier that has a gain of -4V/V. Assume that the MOSFET has K_n=1 mA/V^2 and V_{Th}=1V.

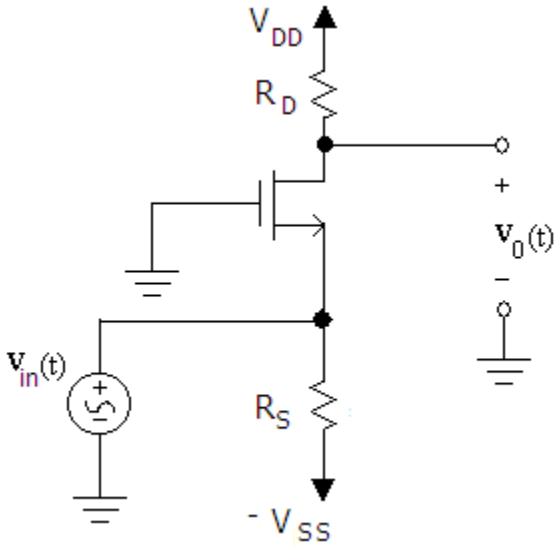
24. Determine the voltage gain and current gain of the variation of the source follower circuit shown below. Assume K_n=1mA/V^2, and V_{Th}=1V.



25. Determine the small signal parameters of voltage gain, input resistance and output resistance of the following circuit. Assume K_n=0.2 mA/V^2, and V_{Th}=1V.

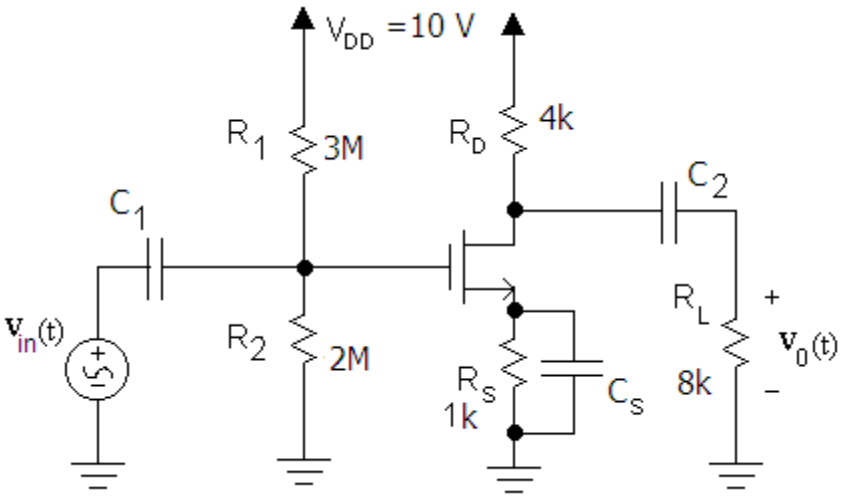


26. Draw the small signal equivalent circuit of the "common gate amplifier" shown below.

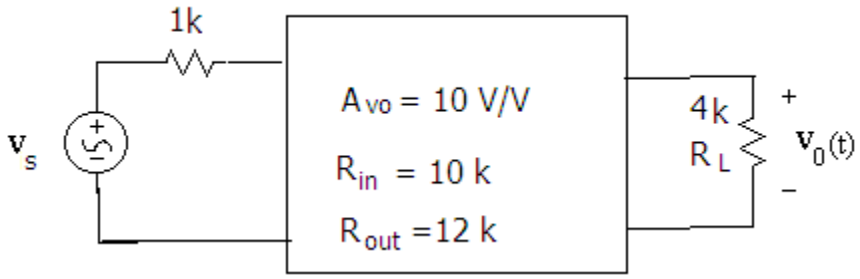


27. Derive the expressions for A_{VO}, R_{in}, and R_{out} for the "common gate amplifier" shown above. Derive the expression in terms of g_m and the labeled resistors.

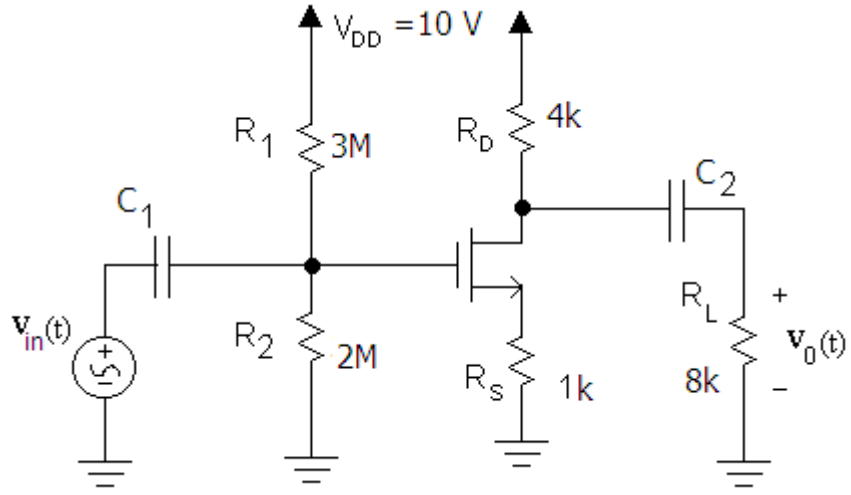
28. Find the voltage amplifier model of the circuit below (with the load removed) by determining the small signal parameters of voltage gain (A_{vo}), input resistance (R_{in}), and output resistance (R_{out}). Using this model, find the voltage gain of the circuit with the load attached. Assume K_n=1mA/V^2, and V_{Th}=1V.



29. If an amplifier with voltage amplifier parameters of A_{vo}=10 V/V, R_{in} = 10k, and R_{out}=12k is connected to the circuit below, determine the voltage gain of the circuit $A_v=v_o/v_s$.



30. Find the voltage amplifier model of the circuit below (with the load removed) by determining the small signal parameters of voltage gain (A_{vo}), input resistance (R_{in}), and output resistance (R_{out}). Using this model, find the voltage gain of the circuit with the load attached. Assume K_n=1mA/V^2, and V_{Th}=1V. Note that there is no bypass capacitor across the source resistance! Otherwise, this is the same circuit as that in problem 26.



31. Using the Java Circuit Simulator, determine the drain current for the circuit shown in problem 10. Be sure that you adjust the MOSFET parameters (Beta and Vth) to the values give in the problem and note that Beta=2Kn.

32. Using the Java Circuit Simulator, verify the answer for Example 4. Be sure that you adjust the MOSFET parameters (Beta and Vth) to the values give in the problem and note that Beta=2Kn.

33. Using the Java Circuit Simulator, simulate the circuit shown in Example 5. Use a potentiometer for R_D and then verify the answer by using the adjusting the potentiometer to obtain the desired drain current I_D. Be sure that you adjust the MOSFET parameters (Beta and Vth) to the values give in the problem and note that Beta=2Kn.

34. Using the Java Circuit Simulator, determine the gain of the common source amplifier from Example 14. Be sure that you adjust the MOSFET parameters (Beta and Vth) to the values give in the problem and note that Beta=2Kn.

Chapter 4: Bipolar Junction Transistors

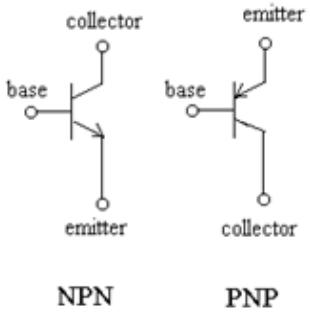
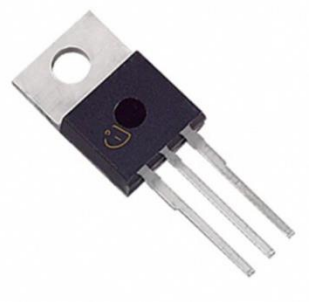
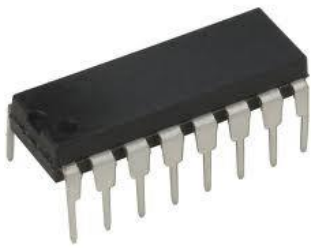
Introduction

The bipolar junction transistor (BJT) is an electronic device that is used in both amplifiers and electronic switches. BJTs were invented around 1949 (before MOSFETs) and replaced the vacuum tube in a variety of applications. Compared to vacuum tubes, BJTs are vastly smaller, consume far less energy, cheaper, and are much more reliable. BJTs made it possible to construct computers that were smaller than an elephant. Because of these advantages, vacuum tubes are almost extinct with the only remaining application being in high end audio amplifiers where many audiophiles prefer them to BJT or MOSFET based amplifiers.

Compared to MOSFETs, BJTs are:

- Generally faster in switching applications than MOSFETs.
- More rugged, because MOSFETs can be destroyed by static electricity.
- Less energy efficient.
- Generally less density possible on an IC compared to MOSFETs

There are two types of BJTs, the NPN and the PNP. We will focus primarily on the NPN BJT although the same fundamental concepts apply to both types. The circuit symbol for NPN and PNP transistors are shown in Figure 36. Like MOSFETs, BJTs can be discreet (see Figure 87) or be embedded into an integrated circuit (see Figure 88).

Schematic Symbols for BJT	Discreet BJT	IC containing BJTs
 Figure 86: Schematic Symbols for BJTs	 Figure 87: TIP 120 BJT	 Figure 88: BJT Transistor Array Integrated Circuit

Simplified Construction and Operation of an NPN Transistor

A greatly simplified version of the construction of an NPN transistor is shown below. Examining the base and emitter terminals we find the PN junction that has the same i-v characteristics as that found in the common junction diode.

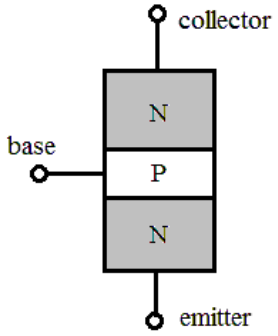


Figure 89: Physical Construction of an NPN Transistor

For instance, if we place a voltage source across these terminals (v_{BE} in Figure 90) we find the familiar exponential relationship (Shockley Equation) between the voltage across this junction and the current through it (see Figure 91). Rather than use the Shockley equation we will use the common voltage drop model and assume that it takes about 0.7 volts to "turn on" the transistor (i.e. to cause current to flow into the base).

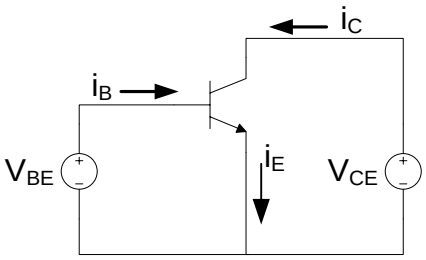


Figure 90: Circuit Illustrating Relationship Between i_B and v_{BE}

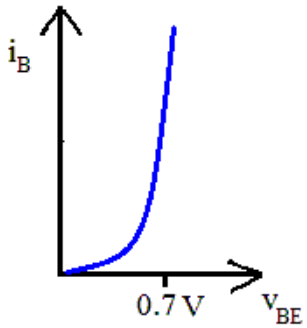


Figure 91: Graph of i_B vs. v_{BE}

When current enters the base of the transistor this allows current to flow into the collector (i_C). From KCL, the emitter current must equal the sum of the base and collector currents.

$$i_E = i_B + i_C$$

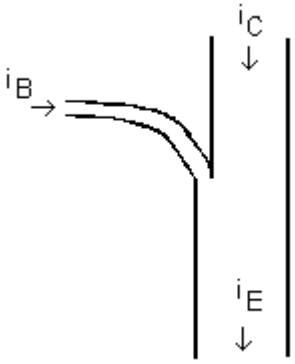


Figure 92: $i_E=i_B+i_C$

The base current can be thought of as the "control" current for the transistor. If no base current is present, then no collector current can flow. Assuming a base current is present and the voltage $V_{CE} \geq V_{BE}$ the graph of the collector current will be exponential and will be greater (typically 100 times or more) than the base current. Although when $V_{CE} \geq V_{BE}$ would appear to reverse bias the base collector junction resulting in no current flow, the construction of the transistor is asymmetric and as a result this junction does not behave as a typical diode would. The relationship between v_{BE} and i_C can be described using the simplified Shockley equation:

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}$$

Note that the collector current is controlled by the base to emitter voltage.

Modes of Operation

Like the MOSFET, the BJT has three distinct modes of operation. These modes are called cutoff, saturation, and active. These modes are analogous the MOSFET modes of cutoff, triode, and saturation respectively. Note that it is the BJTs saturation mode that is analogous to the MOSFET triode mode not the MOSFET saturation mode!

We will illustrate these modes and the operation of an NPN BJT with a conceptual experiment. In the experiment, we apply variable voltages from base to emitter and from collector to emitter as shown in Figure 93 below and note the resulting currents.

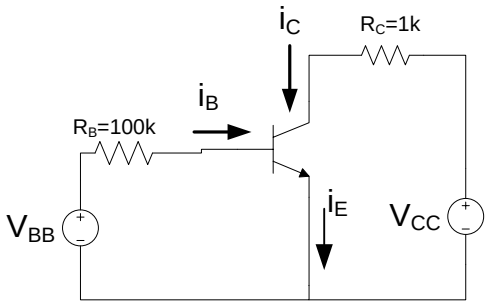


Figure 93: Modes of Operation

Cutoff Mode

We begin the experiment by setting v_{BB}=0. When v_{BB}=0, no current flows into the base and as a result the collector current i_C is also zero. As stated earlier, the base emitter junction acts as a diode and very little base current flows until the base-emitter voltage (v_{BE}) reaches about 0.7 V. For v_{BE}<0.7 V the transistor is said to be in cutoff mode and all currents are close to zero. Therefore, we can use the circuit model shown in Figure 94 to represent a BJT in cutoff mode. Note the open circuits between each of the terminals.

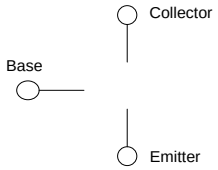


Figure 94: Cutoff Model

$$Cutoff\ Conditions\text{:}\ v_{BE} < 0.7\ V$$

Active Mode

If we set V_{BB} above 0.7 V, current will flow into the base. For illustration purposes, we will set V_{BB}=2.7 V which will make the math easy. Because the base emitter junction behaves as a diode the voltage drop across this junction will be approximately 0.7 V (alternately, we could the Shockley equation but this would make the analysis more cumbersome with little increase in accuracy). Using KVL we determine the voltage drop across the resistor.

$$V_{BB} - V_{R_B} - V_{BE} = 0$$

$$V_{R_B} = V_{BB} - V_{BE}$$

$$V_{R_B} = 2.7 - 0.7 = 2\ V$$

We find I_B using Ohm's Law:

$$I_B = \frac{2}{100\text{k}} = 20\ \mu\text{A}$$

If we gradually increase V_{CC}, and measure the resulting collector current i_C, we obtain a graph similar to that shown in Figure 95 below. Note that for V_{CE}>0.2 V, the collector current is constant and is much greater than the base current.

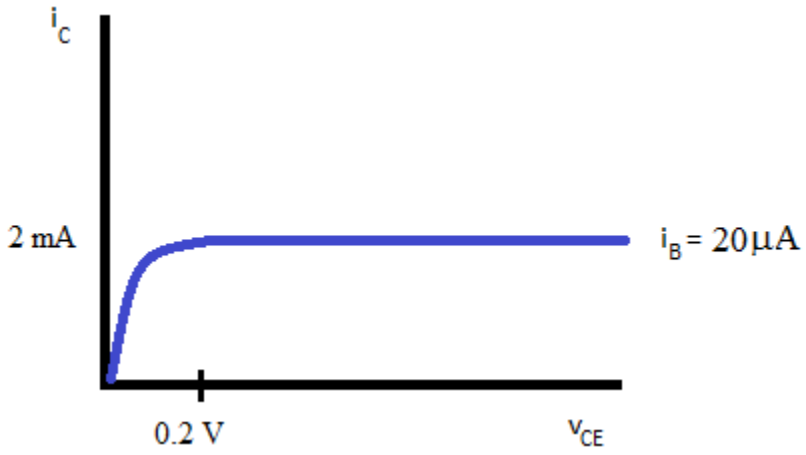


Figure 95: i_C vs. v_{CE}

If we repeat this experiment for V_{BB}=4.7 V and V_{BB}=6.7 V, resulting in I_B=40 µA and I_B=60 µA, and plot the results on a single graph, we would obtain the family of curves shown in Figure 96.

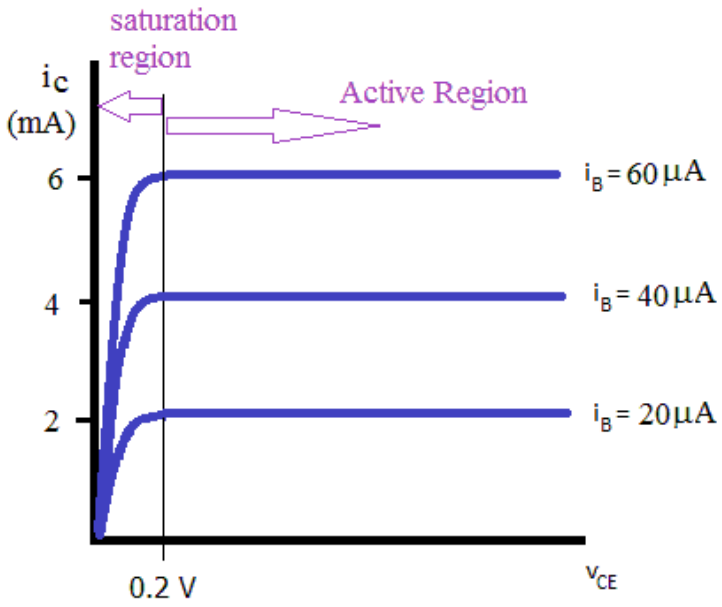


Figure 96: i_C vs. v_{CE} Curves for Several Base Currents

Note that for V_{CE}>0.2 V, the relationship between i_B and i_C is linear. We can write

$$i_C = \beta i_B$$

where β is the current gain for the transistor. Typical values of β are between 50 and 300. Examining the graph above, we see that for this transistor β=100.

The transistor is said to be in the *active* mode for values of V_{CE}>0.2 V. The circuit model shown in Figure 97 describes the behavior of a BJT in the active mode.

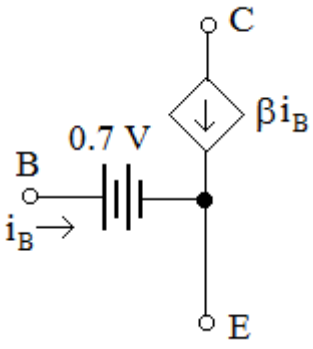


Figure 97: Active Model

$$Active\ Conditions:\ v_{CE} > 0.2\ V\ \textbf{and}\ i_B > 0$$

Because i_B, i_C, and i_E are related by KCL we can derive the relationship between i_C and i_E as follows.

$$i_E = i_B + i_C$$

$$i_C = \beta i_B$$

$$i_E = \frac{\beta + 1}{\beta}\, i_C$$

We define

$$\alpha = \frac{\beta}{\beta + 1}$$

Therefore

$$i_C = \alpha i_E$$

Saturation Mode

Saturation occurs for small values of v_{CE}. When v_{CE}<0.2 V, the active mode relationship $i_C = \beta i_B$ is no longer true as evident in the graph of Figure 95. When the transistor is in saturation, the collector current will be less than that for the active region. The circuit model for the saturation mode is shown in Figure 98.

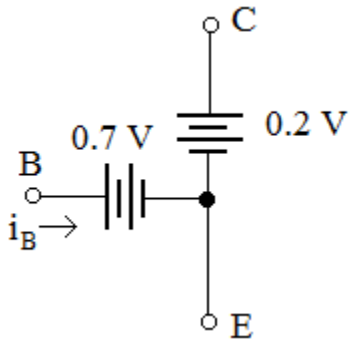


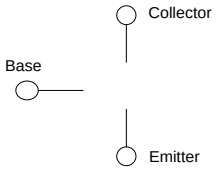
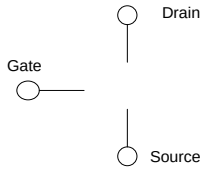
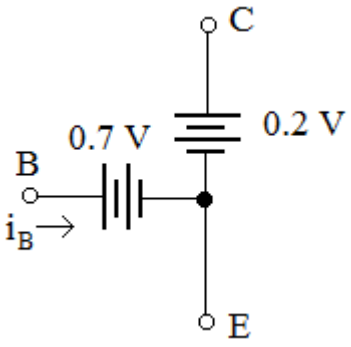
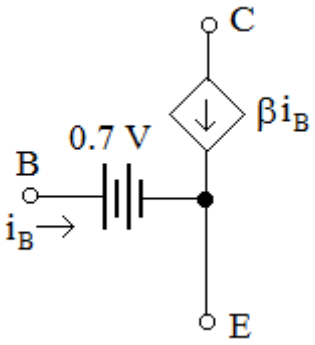
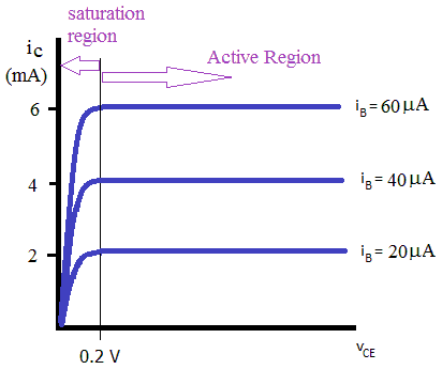
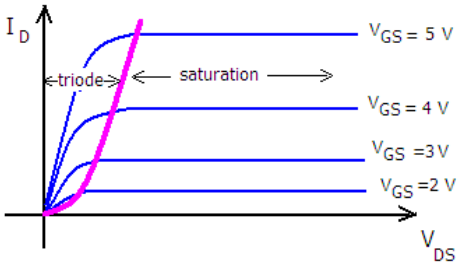
Figure 98: Saturation Model

$$Saturation\ Conditions:\ I_C < \beta I_B\ \ \textbf{and}\ i_B > 0$$

Note that we approximate both the base emitter junction and collector emitter junction as providing a constant voltage drop. We could use a second order equation (as was done with the MOSFET in the triode region) to more accurately describe the dependence of v_{CE} on i_C in the saturation region. However, this would be more difficult to apply and yield only a small increase in accuracy. The circuit model above provides a good balance between accuracy and ease of use.

Comparison of Modeling Approaches of MOSFETs and BJTs

We model the behavior of transistors in order to analyze transistor based circuits. With MOSFETs we developed methods to analyze both DC and AC (small signal) circuits. For DC circuits, we used mathematical equations to describe the relationship between the drain current I_D and the control voltage V_{GS}. We did this because the relationship was non-linear – for both the triode and saturation regions. With BJTs on the other hand, the relationship between the collector current i_C and the control current i_B is linear ($i_C=\beta i_B$) and we can therefore use a linear circuit model – the current controlled current source. For the saturation region (analogous to the MOSFETs triode region) we have also created a linear model where the voltage V_{CE} is approximated with a constant voltage of 0.2 V. Although this is rough approximation, the voltages involved are quite small so that there is very little loss of accuracy assuming the voltages in the circuit are large in comparison. The table below summarizes the DC approaches to analyzing transistor circuits. Later we will introduce small signal model for the BJT and compare it with the MOSFET model.

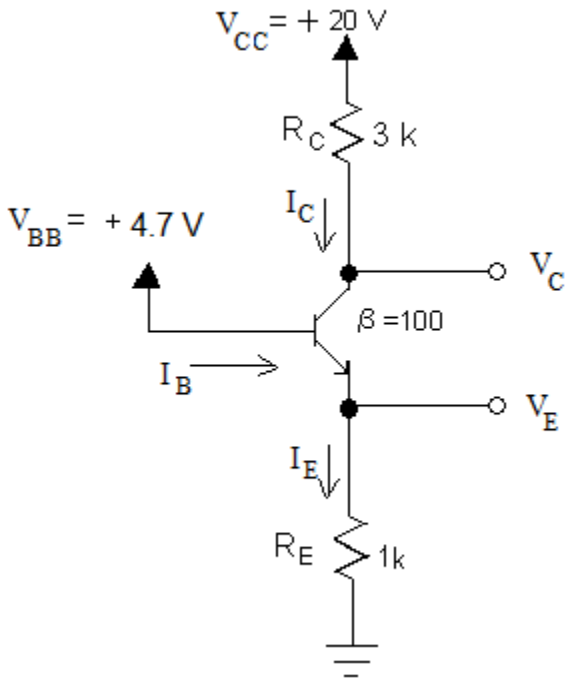
	BJT	MOSFET
"Switch Off" Mode BJT: Cutoff MOSFET: Cutoff	Cutoff 	Cutoff 
"Switch On" Mode BJT: saturation MOSFET: triode	Saturation 	Triode $i_D = K_n[2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2]$ $i_G = 0$
"Amplifier" Mode BJT: Active MOSFET: Saturation	Active 	Saturation $i_D = K_n(v_{GS} - V_{Th})^2$ $i_G = 0$
		

DC Analysis of NPN Circuits

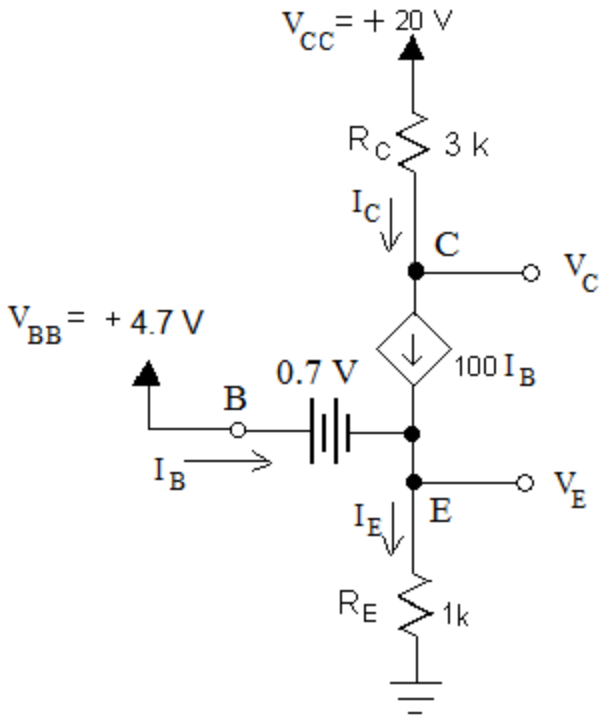
To analyze NPN - BJT circuits we first assume a mode of operation; we then calculate the currents and voltages in the circuit; and finally verify that our assumption was correct. If our assumption is proved false, we will need to reanalyze the circuit based upon a different assumption. For instance, if we assume a BJT is operating in the active region, we will need to calculate the base current to make sure it is a positive value, and determine the voltage V_{CE} to make sure it is greater than 0.2 V.

Example 19: BJT in Active Region

Determine the mode of operation, the currents I_B, I_C, and I_E, and the Voltages V_B, V_C and V_E.



We begin by assuming the transistor is operating in the active region. The original circuit with the active mode model for the transistor inserted is shown below.



Using KVL we can write:

$$V_{BB} - V_{BE} - I_E R_E = 0$$
$$4.7 - 0.7 - I_E \times 1k = 0$$
$$I_E = 4\,mA$$

Next we determine I_C and I_B.

$$i_E = \frac{\beta + 1}{\beta}\, i_C$$
$$I_C = \frac{\beta}{\beta + 1}\, I_E = 3.96\,mA$$
$$I_B = \frac{I_C}{\beta} = 39.6\,\mu A$$

We find the terminal voltages using KVL.

$$V_C = V_{CC} - I_C R_C$$
$$V_C = 20 - 3.96\text{m} \times 3\text{k}$$
$$V_C = 8.12\,\text{V}$$

$$V_E = I_E R_E$$

$$V_E = 4\text{m} \times 1\text{k}$$

$$V_E = 4\ \text{V}$$

By inspection: $V_B = 4.7\ \text{V}$

We have determined all of the terminal voltages and currents under the assumption that the transistor was operating in the active region. We verify the assumption by checking the base current and the collector to emitter voltage are valid. The value of V_{CE} is:

$$V_{CE} = V_C - V_E = 4.12\ V$$

$$I_B > 0 \quad \surd$$

$$V_{CE} > 0.2\ V \quad \surd$$

Since both of the required conditions for active mode operation are correct, the transistor is indeed operating in the active mode and the voltages and currents calculated above are correct.

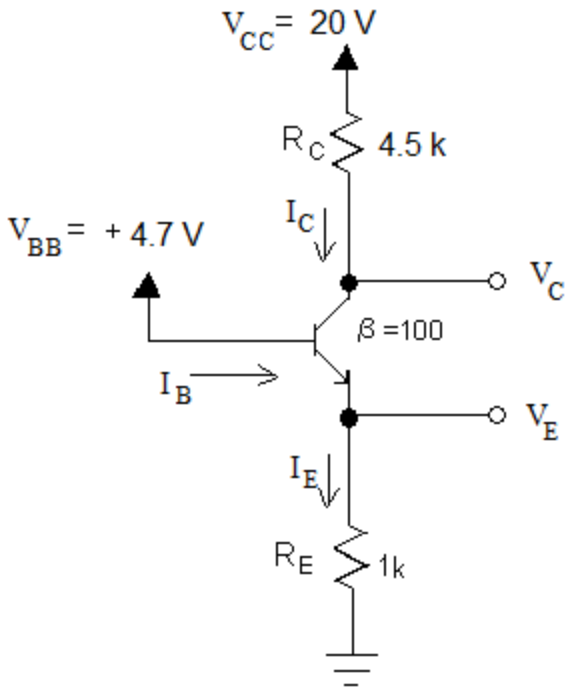
Answers:

$$I_B = 39.6\ \mu A, \quad I_C = 3.96\ mA, \quad I_E = 4\ mA$$

$$V_B = 4.7\ V, \quad V_C = 8.12\ V, \quad V_E = 4\ V$$

Example 20: BJT in Saturation

Determine the mode of operation, the currents I_B, I_C, and I_E, and the Voltages V_B, V_C and V_E.

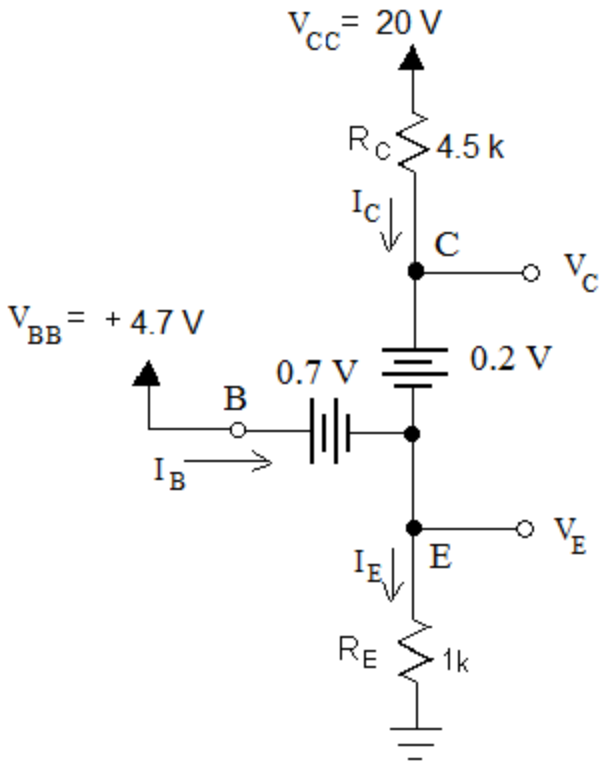


This is the same problem as the previous example except that R_C has increased to 4.5 kΩ. The calculations for the currents remain the same as the previous problem as do the voltages V_B and V_E. The value of V_C however will need to be recalculated.

$$V_C = V_{CC} - I_C R_C$$
$$V_C = 20 - 3.96\text{m} \times 4.5\ \text{k}$$
$$V_C = 2.18\ \text{V}$$

$$V_{CE} = V_C - V_E = -1.82\ V$$

Since V_{CE}<0.2, the active mode assumption is invalid. Since the current I_B is positive, indicating that the transistor in not in cutoff, we shall assume the transistor is in saturation mode and analyze the circuit based on this assumption. The saturation mode equivalent circuit is shown below.



Using KVL we find V_E and V_C.

$$V_E = 4.7 - 0.7 = 4\ V$$

$$V_C = 4 + 0.2 = 4.2\ \text{V}$$

Using Ohm's Law we find the transistor currents.

$$I_E = \frac{\text{V}_\text{E}}{\text{R}_\text{E}} = \frac{4}{1\text{k}} = 4\ \text{mA}$$

$$I_C = \frac{\text{V}_\text{CC} - V_C}{\text{R}_\text{C}} = \frac{20 - 4.2}{4.5\ \text{k}} = 3.51\ \text{mA}$$

$$I_B = I_E - I_C = 4\ - 3.51 = 49\ \mu A$$

Next we check the saturation assumption.

$$I_B > 0 \quad \surd$$

$$I_C < 100\ \text{I}_\text{B} \quad \surd$$

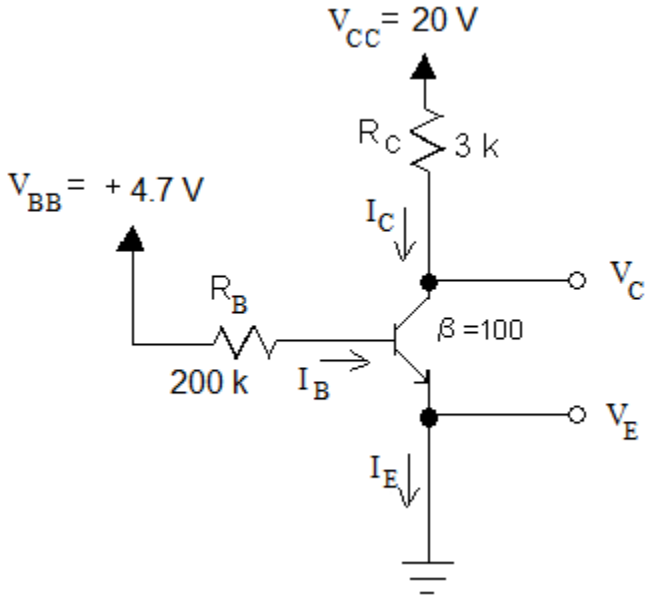
Answers:

$$I_B = 49\ \mu A, \quad I_C = 3.51\ mA, \quad I_E = 4\ mA$$

$$V_B = 4.7\ V, \quad V_C = 4.2\ V, \quad V_E = 4\ V$$

Example 21: BJT with Base Resistor

Determine the mode of operation, the currents I_B, I_C, and I_E, and the Voltages V_B, V_C and V_E.



We begin by assuming the transistor is operating in the active region. (Rather than redrawing the circuit with the model inserted as we have done previously, we will mentally place the model in the circuit.)

Using KVL we can write:

$$V_{BB} - I_B R_B - V_B = 0$$

$$I_B = \frac{\mathrm{V_{BB}} - V_B}{\mathrm{R_B}} = \frac{4.7 - 0.7}{200\ \mathrm{k}} = 20\ \mu\mathrm{A}$$

Since we have assumed active region: $I_C = \beta I_B$

$$I_C = 100 \times 20\mu = 2\ \mathrm{mA}$$

From KCL we find: $I_E = I_B + I_C = 2.02\ mA$

Now we determine V_C.

$$V_C = V_{CC} - I_C \times R_C = (20) - (2\mathrm{m})(3\mathrm{k}) = 14\ \mathrm{V}$$

Next we check our active mode assumption. Since the emitter terminal is at ground, $V_{CE} = V_C = 14$ V.

$$I_B > 0 \quad \surd$$

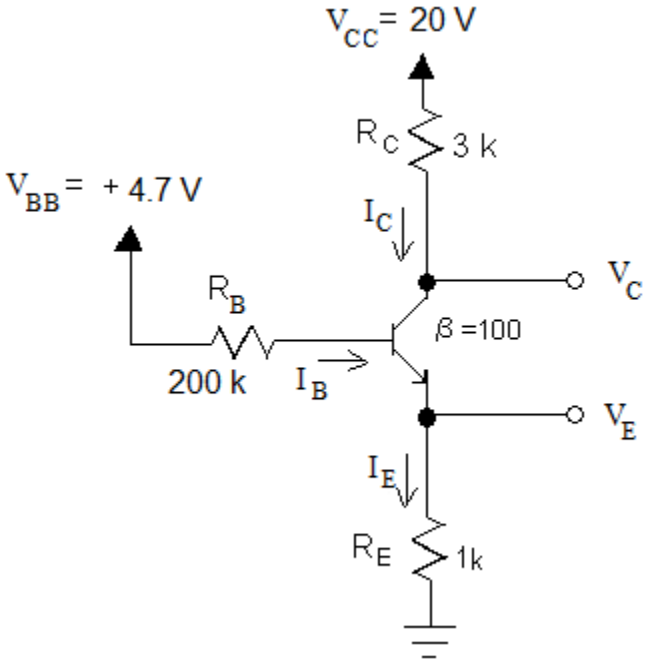
$$V_{CE} > 0.2\,V \quad \surd$$

Answers:

$$I_B = 20\ \mu A, \quad I_C = 2\ mA, \quad I_E = 2.02\ mA$$
$$V_B = 0.7\ V, \quad V_C = 14\ V, \quad V_E = 0\ V$$

Example 22: BJT with R_B and R_E

Determine the mode of operation, the currents I_B, I_C, and I_E, and the Voltages V_B, V_C and V_E.



We begin by assuming the transistor is operating in the active region. Using KVL we write. Using KVL we can write:

$$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$$

From $I_E = I_B + I_C$ and $I_C = \beta I_B$ we can write:

$$I_E = (\beta + 1) I_B$$

Substituting this equation into the KVL equation we find:

$$V_{BB} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$I_B = \frac{4.7 - 0.7}{200\text{k} + (100 + 1)1\text{k}} = 13.3\ \mu A$$

$$I_C = \beta I_B = 1.33\ \text{mA}$$

$$I_E = I_B + I_C = 1.35\ \text{mA}$$

Next we calculate the terminal voltages:

$$V_C = V_{CC} - I_C \times R_C = (20) - (1.33\text{m})(3\text{k}) = 16\ \text{V}$$

$$V_E = I_E \times R_E = (1.35\text{m})(1\text{k}) = 1.35\ V$$

$$V_B = V_E + V_{BE} = 1.35 + 0.7 = 2.05\ \text{V}$$

Next we check our active mode assumption.

$$V_{CE} = V_C - V_E = 16 - 1.35 = 14.65V$$

$$I_B > 0 \quad \surd$$

$$V_{CE} > 0.2\ V \quad \surd$$

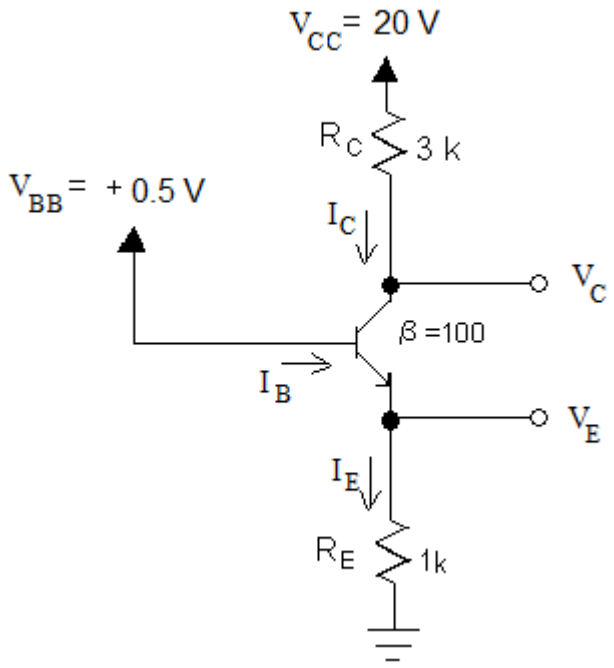
Answers:

$$I_B = 13.3\ \mu A, \quad I_C = 1.33\ mA, \quad I_E = 1.35\ mA$$

$$V_B = 2.05\ V, \quad V_C = 16\ V, \quad V_E = 1.35\ V$$

Example 23: BJT in Cutoff

Determine the mode of operation, the currents I_B, I_C, and I_E, and the Voltages V_B, V_C and V_E.



We begin by assuming the transistor is operating in the active region. Using KVL we write. Since VB=0.5 and VBE=0.7, then VE=-0.2V

$$I_E = \frac{V_E}{R_E} = \frac{-0.2}{1\text{k}} = -0.2 \text{ mA}$$

From $I_E = I_B + I_C$ and $I_C = \beta I_B$ we can write:

$$I_B = \frac{I_E}{\beta + 1} = \frac{-0.2}{100 + 1} = -1.98 \text{ μA}$$

A negative answer for I_B indicates that the transistor is not operating in the active mode. We will assume that the transistor is operating in cutoff. In cutoff we find:

$$I_B = I_C = I_E = 0 \quad \text{and therefore } V_C = 20 \text{ V} \quad V_E = 0 \quad V_B = 0.5 \text{ V}$$

To check for cutoff:

$$V_{BE} < 0.7\,V \quad \surd$$

The PNP Transistor

The PNP transistor consists of a layer of N material surrounded by P material. This construction results in a device that requires opposite voltage polarities to be applied than that of the NPN transistor. These opposite voltage polarities result in current directions that are the opposite of

the NPN. The result is that we can use the same analysis techniques and formulas developed with the NPN but we must replace v_{BE} with v_{EB} in the formulas and reverse all current directions. For PNP transistor, the voltage at the emitter must be higher than the base (by about 0.7 V) or else it is in cutoff mode. Voltage at emitter must be higher than the collector by at least 0.2V or the transistor will be in saturation mode. The models for active mode and saturation are shown in Figure 99 and Figure 100 respectively.

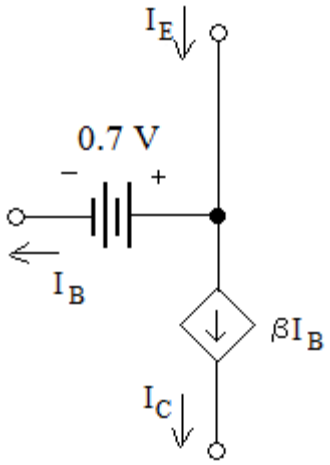


Figure 99: PNP Active Mode Circuit Model

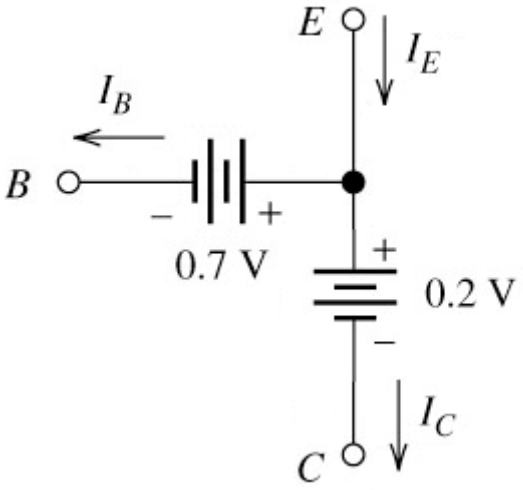
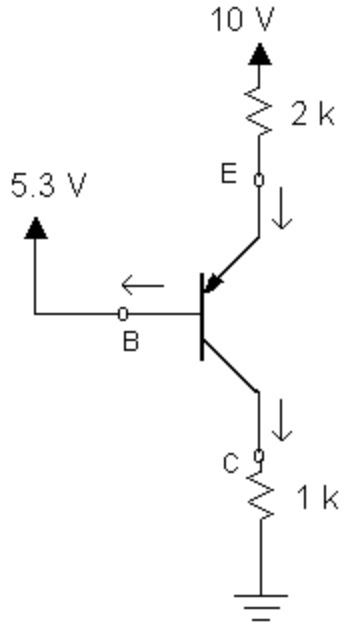


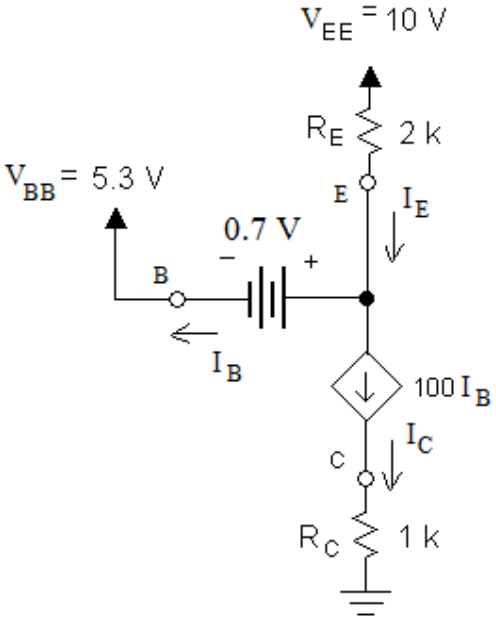
Figure 100: PNP Triode Circuit Model

Example 24: PNP in Active Region

Determine the mode of operation, the currents I_B, I_C, and I_E, and the Voltages V_B, V_C and V_E. Assume β=100.



We begin by assuming the transistor is operating in the active region. The original circuit with the active mode model for the transistor inserted is shown below.



We begin by noting by inspection that $V_B = 5.3$ V and $V_E = 6$ V. (V_E=V_B+0.7)

Next we determine I_E using Ohm's Law.

$$I_E = \frac{V_{EE} - V_E}{R_E}$$

$$I_E = \frac{10 - 6}{2k} = 2\ mA$$

Next we determine I_C and I_B.

$$I_C = \frac{\beta}{\beta + 1}\ I_E = 1.98\ mA$$

$$I_B = \frac{I_C}{\beta} = 19.8\ \mu A$$

We find the terminal voltages using KVL.

$$V_C = I_C R_C$$

$$V_C = 1.98\text{m} \times 1\text{k}$$

$$V_C = 1.98\ \text{V}$$

We have determined all of the terminal voltages and currents under the assumption that the transistor was operating in the active region. We verify the assumption by checking the base current and the collector to emitter voltage are valid. The value of V_{EC} is:

$$V_{EC} = V_E - V_C = 6.02\ V$$

$$V_{EC} > 0.2\ V \quad \surd$$

$$I_B > 0 \quad \surd$$

Since both of the required conditions for active mode operation are correct, the transistor is indeed operating in the active mode and the voltages and currents calculated above are valid.

Answers:

$$I_B = 19.8\ \mu A, \quad I_C = 1.98\ mA, \quad I_E = 2\ mA$$

$$V_B = 5.3\ V, \quad V_C = 1.98\ V, \quad V_E = 6\ V$$

Load Line Analysis

Load line analysis provides good insights into how circuit parameters effect circuit operation. For instance, we may be interested in seeing what effect adjusting the collector resistor has on the mode of operation in the circuit shown in Figure 101.

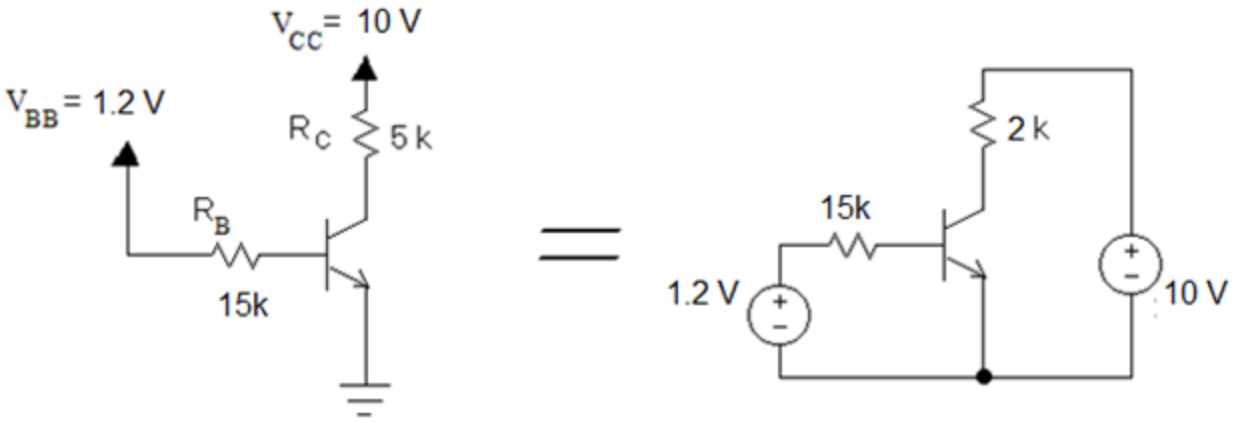


Figure 101: Load Line Analysis

As we did with MOSFETs, we plot the load line of the of the source/resistor combination (1.2 V/15k) on the "input side" of the transistor on the graph of the i_B vs. v_{BE} characteristic curve. The intersection of these curves is the operating point. We see from the graph that the approximate base current is 40µA. We then plot the right hand side resistor/source combination (10 V/5k) on the i_C vs. v_{CE} characteristic curve. The intersection of the load line with the previously determined base current reveals the operating point. For this circuit, the base current was found to be 40 µA so the intersection of this curve with the load line plot reveals the operating point on the "output side" of the transistor. As seen from the graph, the operating point is:

$$i_C \cong 4\,mA \qquad v_{CE} \cong 2V$$

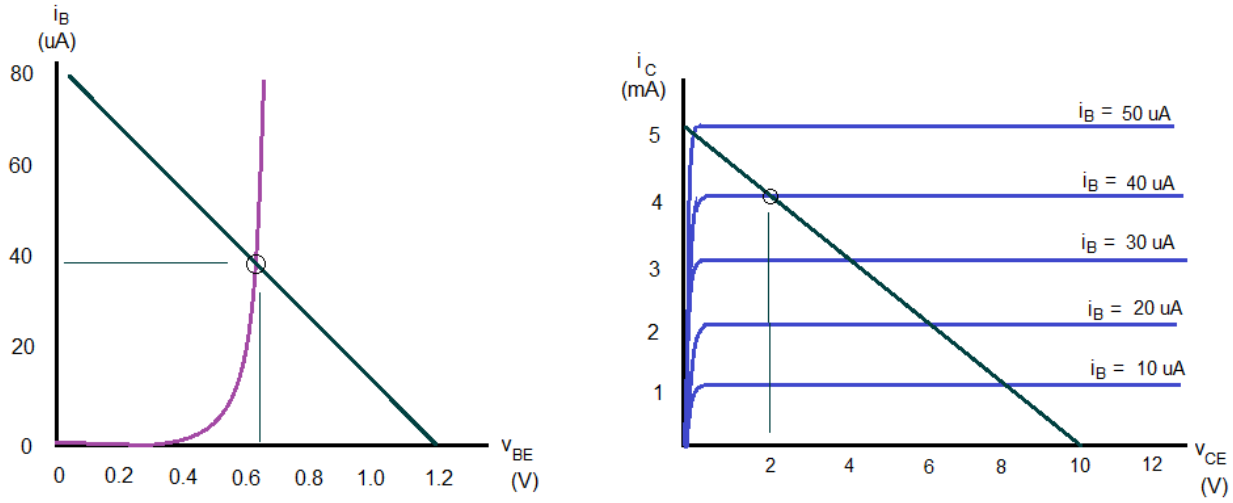


Figure 102: Load Line Characteristic Curves

We can see from these graphs how circuit parameters affect the circuit performance. For instance, on the input side of the transistor, decreasing R_B will make move the operating point up the characteristic curve because the load line slope will increase. The result will be an increased base current. On the output side of the transistor, we see that increasing the base current tends to move the transistor toward saturation. With an increased base current, if we want to keep the transistor in the active mode, we would need to either increase V_{CC} or decrease R_C.

BJT as a switch

BJTs can be used as current controlled switches. The cutoff mode is used as the off condition and the saturation mode is typically used for the on condition. The saturation mode is used because this will minimize the voltage drop across the collector-emitter junction. In an ideal switch, this voltage drop would be zero. We will examine two applications, a logic inverter and a motor control circuit.

Logic Inverter

The BJT logic circuit uses the cutoff and saturation modes. Typically 5 V is used to represent high signals and 0 V low signals. For the inverter configuration shown in Figure 103, when V_{in} is low no current will flow into the base and the transistor is in cutoff mode and consequently the value of V_{out} will be V_{CC}. If V_{in} is high, current will flow into the base. If R_B and R_C are selected appropriately, the transistor will be in saturation mode and V_{out} will be low.

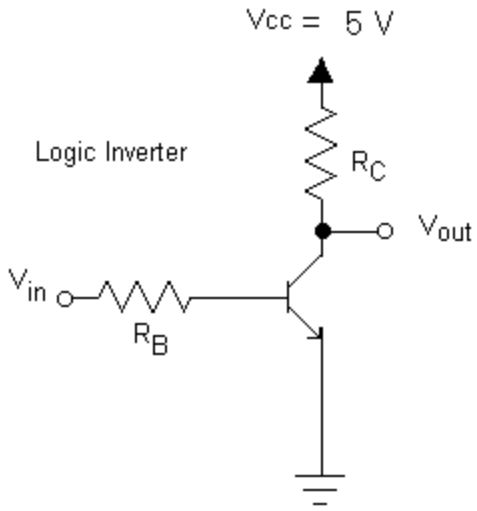


Figure 103: Logic Inverter Circuit

Example 25: Analysis of a Logic Inverter

Plot the transfer characteristic v_{out} vs. v_{in} for the circuit in Figure 103 if R_B=10 kΩ, R_C=500 Ω, and β=100. Repeat for β=50 and β=200.

For V_{in}<0.7 V, the transistor will be in cutoff which results in vout =5 V. For V_{in}>0.7 V, the transistor enters the active region, and the vout drops as the collector current rises. We will find the value of V_{in} that places the transistor on the boundary between the active mode and the saturation mode. We can find this value by assuming that $I_C=\beta I_B$ and that v_{out}=0.2 V.

For the active region we find that

$$v_{out} = V_{CC} - i_C \times R_C$$

$$where \quad i_C = \beta i_B \quad and \quad i_B = \frac{(v_{in} - 0.7)}{R_B}$$

$$therefore \quad v_{out} = V_{CC} - \beta \frac{(v_{in} - 0.7)}{R_B} \times R_C$$

Substituting the circuit element parameters given in the problem statement gives us the equation of v_{out} as a function of v_{in} when the transistor is in the active mode.

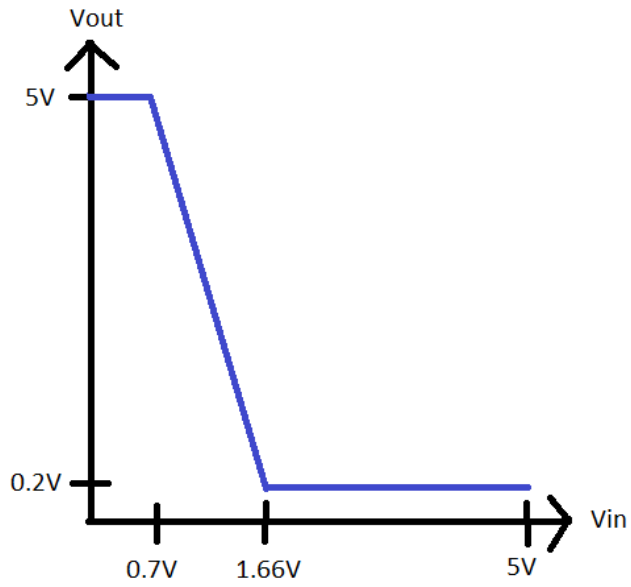
$$v_{out} = 5 - 100 \frac{(v_{in} - 0.7)}{10\text{k}} \times 500$$

$$\text{v}_{\text{out}} = 5 - 5 \times (v_{in} - 0.7)$$

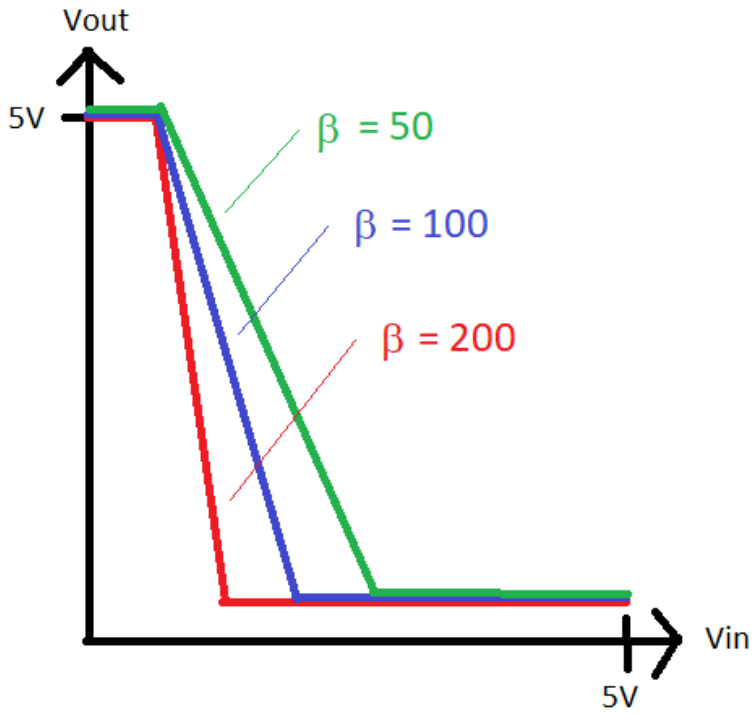
This equation is valid when the transistor is in the active mode. To find the value of v_{in} that that places the transistor on the edge of saturation we set v_{out}=0.2 V and solve for vin. We find that

$$v_{in,eos} = 1.66 \text{ V}$$

For values of v_{in}>1.66 V, the transistor will be in saturation and the value of v_{out}=0.2 V. We are now ready to construct the graph of the transfer characteristics.



We can repeat this process for β=50 and β=200. The results along are shown below.



Simulation: BJT Logic Inverter

Motor Driver Circuit

Motor driver circuits are used to interface a motor with its control circuitry. Typically the control is a microcontroller which does not have the ability to source sufficient current to drive the motor. We can connect the control circuit output to a transistor that acts as a switch and have an external power supply power the motor. A simple motor driver circuit is quite similar in topology to the logic inverter (where R_C is replaced by the motor) and uses the saturation and cutoff modes to turn the motor on and off. To design the circuit to work properly, we need to select R_B to ensure the transistor operates in the saturation mode when the value of v_{in} is high.

The value of β can vary even among transistors of the same type and is also dependent upon the collector current and the operating temperature. Because of the variability of β, engineers employ an "overdrive factor" to ensure that the transistor will be in saturation. The overdrive factor is similar idea to the safety factor employed in civil engineering. In civil engineering, the strength of the material is divided by the safety factor to determine the allowable stress. The beam is then designed large enough so that the applied stress is lower than the allowable stress. Similarly, we divide the nominal β for the transistor by the overdrive factor to produce the forced beta (β_F).

$$\beta_F = \frac{\beta}{Overdrive\ Factor}$$

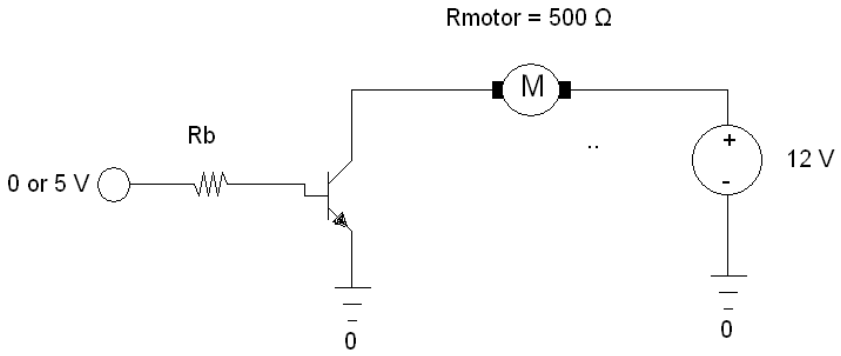
Typical values employed for the overdrive factor are between 2 and 10.

By designing our circuit to operate on the edge of saturation using B_F, the resulting circuit will instead operate safely in the saturation region because the actual value of B is greater than B_F.

Example 26: Design of a Motor Driver

Design a motor driver circuit using a 3904 NPN BJT that will turn on a motor when V_{in}=5 V and turn off the motor when V_{in}=0 V. Assume the motor has a resistance of 500 Ω. The transistor is used because the source that supplies V_{in} is limited to 10 mA and the motor voltage operates at 12 V.

We will use the same circuit topology as that employed by the logic inverter. We will need to select R_B such that the transistor acts in the saturation region when the value of V_{in}=5 V. The circuit will be in cutoff when V_{in}=0 V.



In order to design the circuit we need to find β for this transistor by examining its data sheet which can be found here: http://www.datasheetcatalog.org/datasheet/fairchild/2N3904.pdf. Perusing the datasheet we do not find β listed however we do find a section called "DC Current Gain" with an h_{FE} parameter listed. Instead of using β, datasheets list the current gain as h_{FE} which is a parameter that is used in 2-port equivalent circuits of transistors. We see that rather than give a specific value, a range of values is given and that the range depends upon the collector current. We also see that these values assume a temperature of 25°C. The value of β is a bit harder to determine than we might have expected.

Our first task will be to figure out a reasonable value of β to use as we design our circuit. The design statement specifies R_C =500 Ω. For the on condition, we want the voltage drop across the CE junction to be close to zero. Using Ohm's law we find:

$$I_C = \frac{(V_{CC} - V_{CE})}{R_C} \cong \frac{12 - 0.2}{500} = 23.6\,mA$$

We see that the datasheet lists β (h_{FE}) in a range of 100 to 300. We want the transistor to be in saturation so we will use the "worst case" value of 100. If the actual value is higher, this will tend to drive the transistor deeper into saturation which is acceptable.

From the data sheet we see that the current gain also varies with temperature. To be on the safe side, we will use an overdrive factor to determine a β_F to use in our design. Using an overdrive factor of 2 yields $\beta_F = 50$.

We will find the value of R_B that places the transistor on the edge of saturation assuming that the DC current gain is β_F. The conditions for the edge of saturation are $I_C = \beta_F I_B$ and V_{CE}=0.2 V. Using KVL yields:

$$I_C = \beta_F I_B; \quad I_B = 472\ \mu A$$

$$R_B = \frac{(V_{in} - V_{BE})}{I_B} = \frac{(5 - 0.7)}{472\ \mu} = 9.1\ k\Omega$$

By selecting R_B=9.1 kΩ we ensure that the transistor will operate in the saturation region. The resulting base current I_B of 472 μA is much less than the maximum of 10 mA given in the problem statement.

Bi-directional Motor Control with an H-Bridge

We have already seen how transistors can be used to control motors. We will extend that knowledge to motors that can be operated in forward and reverse directions. The direction of current flow through the motor determines the direction that it will turn so the control circuit must control the direction of current flow in addition to being able to turning the motor on and off. A popular circuit to control bidirectional motors is the “H-bridge” circuit shown in Figure 104 below. If transistors Q1 and Q4 are turned on, the current will flow through the motor to the right. If Q3 and Q2 are on, the current will flow through the motor to the left. We can turn on these transistors using a microcontroller or other control circuitry.

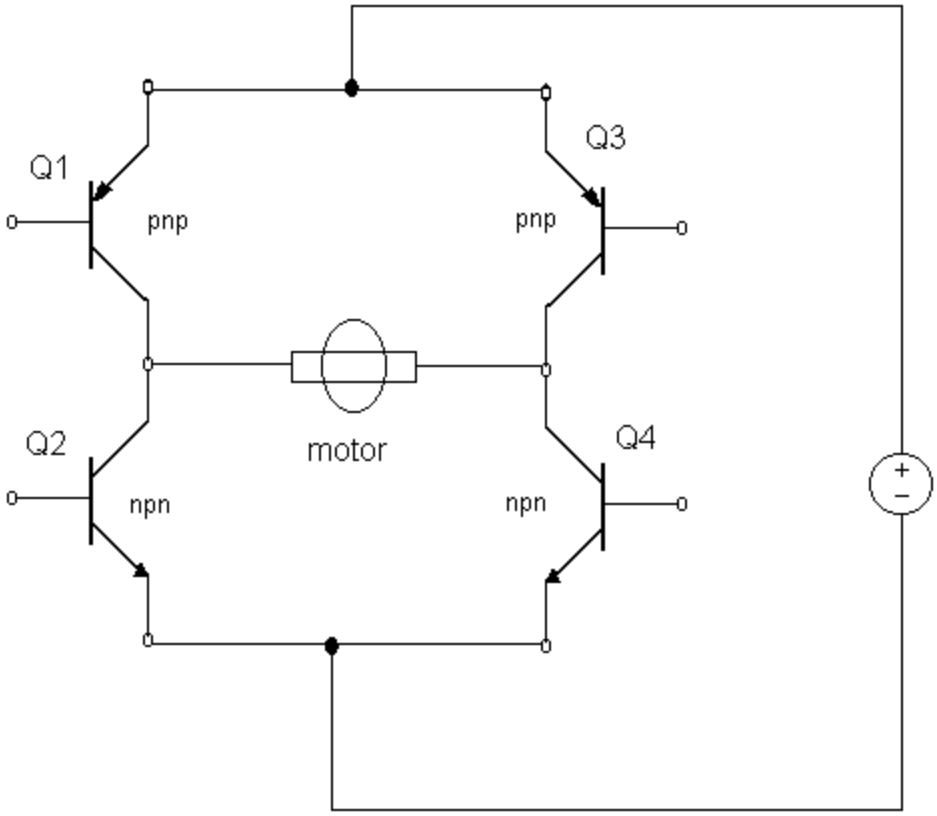


Figure 104: H Bridge Motor Control Circuit

With 4 transistors, there are 16 possible states. Some of the states turn the motor off, some on, some lead to short circuits! Obviously we don't want those states to occur or we may damage the control circuitry attached to the H-bridge. Which states are illegal?

You probably noticed that the transistors Q1 and Q3 are PNP transistors. These are used because the voltage drop across the motor would raise the voltage level at the emitter of Q1 so that it would not be in saturation.

BJT Amplifiers

BJTs can be used to amplify signals. Like the MOSFET, a changing voltage at the input side of the transistor generates changing voltage levels at the output. As an example, refer to the circuit in Figure 105 below. We will use this very simple circuit to illustrate how the transistor can be used to amplify signals.

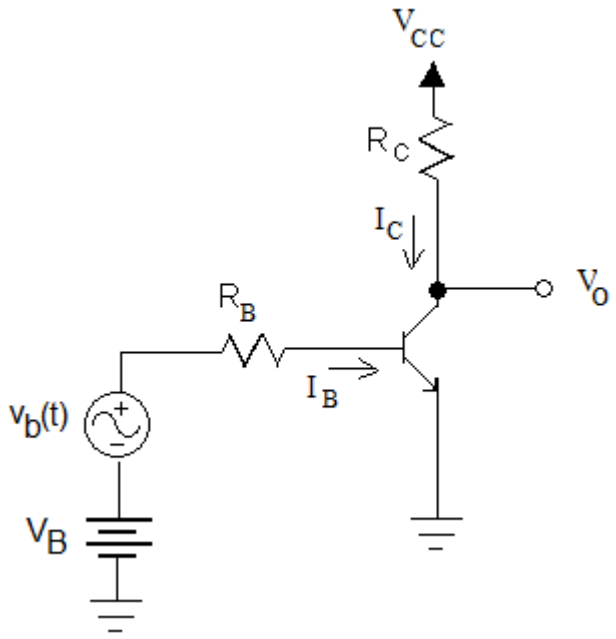


Figure 105: Conceptual Amplifier Circuit

The base voltage consists of a DC voltage V_B and a time varying voltage $v_b(t)$.

$$v_B = V_B + v_b$$

This changing voltage results in a changing base current. The changing base current results in a changing collector current. The changing collector current results in a changing voltage drop across the R_C resistor which results in a changing voltage at the output V_O. Note that as v_B increases, the output voltage decreases since the voltage drop across R_C will be larger for larger collector currents. Next we introduce the small signal parameters for BJTs, develop its small signal model, and apply the model to analyze amplifier circuits.

Small Signal Model

We saw in our analysis of MOSFET amplifier circuits that the small signal model was quite helpful in determining amplifier characteristics such as voltage gain, input resistance, and other parameters. Because typical BJT amplifiers are biased to operate in the active region, we will develop small signal models of the BJT operating in the active mode.

We begin the development of the small signal model of the BJT by referring to its i_C vs. v_{BE} characteristics in the active mode that is described by the Shockley equation.

$$i_C = I_S e^{v_{BE}/V_T}$$

Where the constant V_T is the thermal voltage and I_S is the saturation current.

From this equation we see that the collector current is dependent upon the base to emitter voltage. Compare this to how the MOSFET behaved. A change in the MOSFETs gate to drain voltage induced a change to the drain current. In the MOSFET, we modeled this as a voltage controlled current source. Similarly, for a BJT we can determine a small signal model using the

exponential relationship between the input voltage and the collector current to determine its transconductance.

$$g_m = \left.\frac{di_C}{dv_{BE}}\right|_Q$$

$$g_m = \frac{1}{V_T} I_S e^{V_{BE}/V_T}$$

Since: $$I_{CQ} = I_S e^{V_{BEQ}/V_T}$$

We can write:

$$g_m = \frac{I_{CQ}}{V_T}$$

For MOSFETs no current entered the "input" terminals and therefore the small signal input resistance was infinite. For BJTs a change in input voltage does result in a change in base current (see Figure 91). The small signal input resistance is the inverse of the slope of the i_B vs v_{BE} curve at the DC operating point.

$$r_\pi = \left[\frac{di_B}{dv_{BE}}\right]^{-1}_{v_{BE}=V_{BEQ}}$$

In other words, the small signal input resistance is the slope of the i_B vs. v_{BE} curve at the operating point or quiescent point (Q-point). We can find this resistance in terms of the DC bias current I_{CQ} as follows:

$$i_B = \left[\frac{I_S e^{v_{BE}/V_T}}{\beta}\right]$$

$$\left.\frac{di_B}{dv_{BE}}\right|_Q = \left[\frac{1}{\beta V_T}\left(I_S\, e^{v_{BE}/V_T}\right)\right]_Q$$

$$\left.\frac{di_B}{dv_{BE}}\right|_Q = \left[\frac{1}{\beta V_T}\left(I_S\, (e^{V_{BEQ}/V_T})\right)\right]$$

Since:

$$I_{CQ} = I_S\ (e^{v_{BEQ}/V_T})$$

Then:

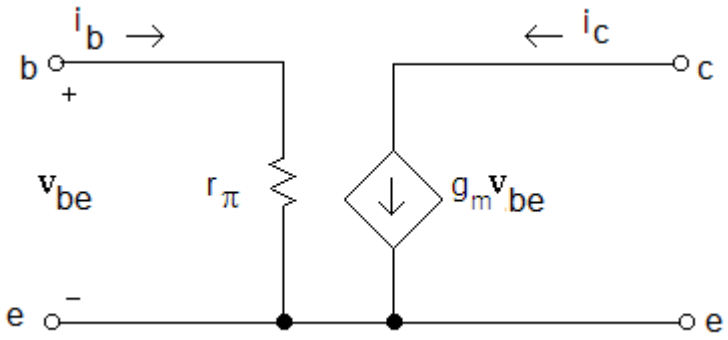
$$\left.\frac{di_B}{dv_{BE}}\right|_Q = \left[\frac{1}{\beta V_T}(I_{CQ})\right]$$

Therefore:

$$r_\pi = \left[\left.\frac{di_B}{dv_{BE}}\right|_Q\right]^{-1} = \left[\frac{I_{CQ}}{\beta V_T}\right]^{-1}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

We can now realize our circuit model as follows using the results for transconductance and input resistance derived above. This model is shown in Figure 106.



$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

Figure 106: BJT Small Signal Model Using g_m

The model above shows that the BJT can be thought of as voltage controlled current source with a finite input resistance. We usually think of the BJT as a current controlled current source and indeed it can be modeled as such. The relationship between the small signal currents i_b and i_c can be derived as follows.

$$i_c = g_m v_{be} \qquad where\ \ v_{be} = i_b r_\pi$$

Therefore:

$$i_c = g_m i_b r_\pi$$

Substituting the equations derived previously for the small signal model yields:

$$i_c = \left(\frac{I_{CQ}}{V_T}\right) i_b \left(\frac{\beta V_T}{I_{CQ}}\right)$$
$$i_c = \beta i_b$$

This is not an unsurprising result as we should have suspected that an increase in the base current would yield an increase in the collector current governed by β.

The resulting small signal model using this result is shown in Figure 107.

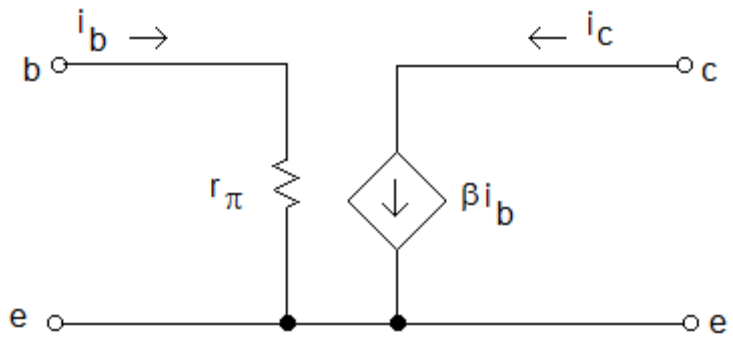


Figure 107: BJT Small Signal Model Using Beta

Either of the models shown in Figure 106 and Figure 107 can be used in small signal analysis of BJT circuits. The choice is a matter of preference.

We can derive a relationship between r_π and g_m by comparing Figure 106 and Figure 107. We note that:

$$i_c = g_m v_{be} = \beta i_b$$

Since $v_{be} = i_b r_\pi$, then:

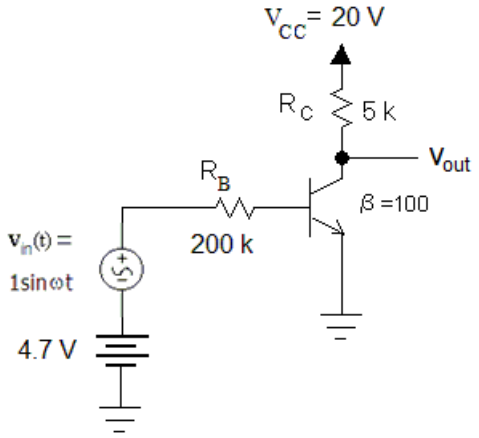
$$g_m = \frac{\beta}{r_\pi}$$

Now that we have a small signal model for the BJT we can analyze amplifier circuits using the following procedure:

4. Use DC analysis to find the DC operating point (Q-point). In particular we must find I_C to determine r_π (and g_m if the transconductance model is desired).
5. Insert the BJT small signal model into the small signal equivalent circuit.
6. Analyze the small signal circuit to find gain and other small signal parameters of interest.

Example 27: Using the Small Signal Model

Determine the small signal voltage gain (v_o/v_{in}) for the circuit below. Assume V_T=26 mV.



In order to find the small signal model we will find the collector current I_{CQ}.

$$I_{BQ} = \frac{4.7 - 0.7}{200\text{ k}} = 0.02\text{ mA}$$

$$I_{CQ} = \beta \times I_{BQ} = 100 \times 0.02\text{m} = 2\ mA$$

Using KVL to calculate the quiescent collector to emitter voltage yields:

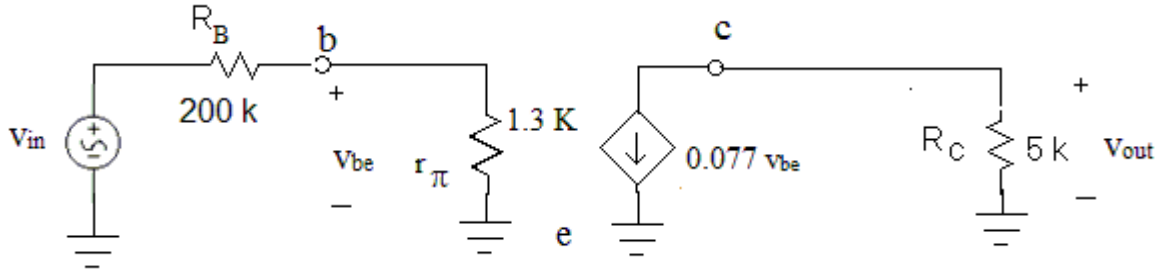
$$V_{CEQ} = 20 - 5k \times 2m = 10\ V$$

Therefore the BJT is indeed operating in the active region ($V_{CE} \geq 0.2$ V and $I_B > 0$). The small signal parameters g_m and r_π can be found using:

$$g_m = \frac{I_{CQ}}{V_T} = \frac{2m}{26m} = 0.077\ A/V$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 26m}{2m} = 1300\ \Omega$$

We now construct the small signal model. Note that the DC voltage sources have been replaced with short circuits (to ground):



To calculate the voltage gain we note that the output voltage is:

$$v_{out} = -g_m v_{be} R_C$$

Where $$v_{be} = v_{in}\left(\frac{r_\pi}{r_\pi + R_B}\right)$$

Substituting v_{be} into the equation above and solving for the voltage gain yields:

$$A_V = -g_m R_C\left(\frac{r_\pi}{r_\pi + R_B}\right)$$

Substituting the parameter values yields:

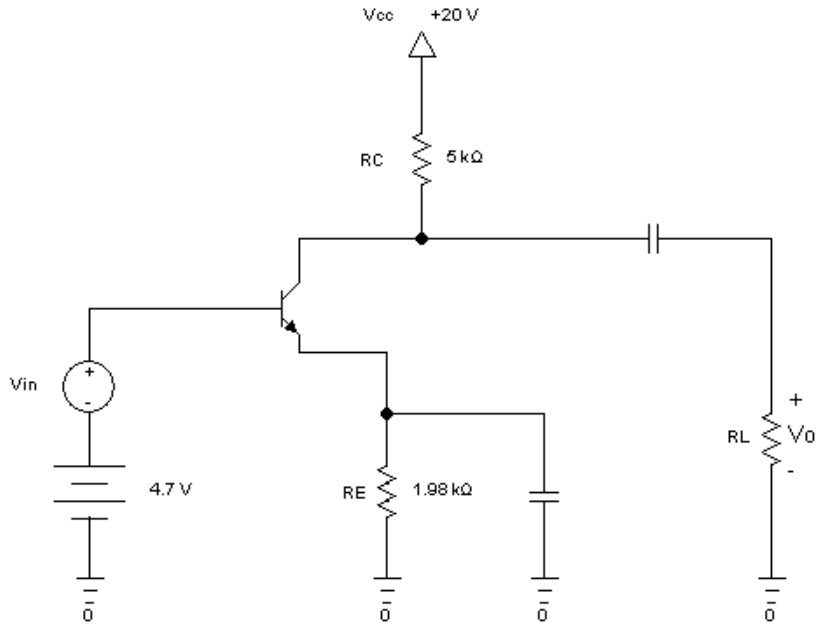
$$A_V = (-0.077)(5\ K)\left(\frac{1.3\ K}{1.3\ K + 200\ K}\right)$$

$$A_V = -2.48\ V/V$$

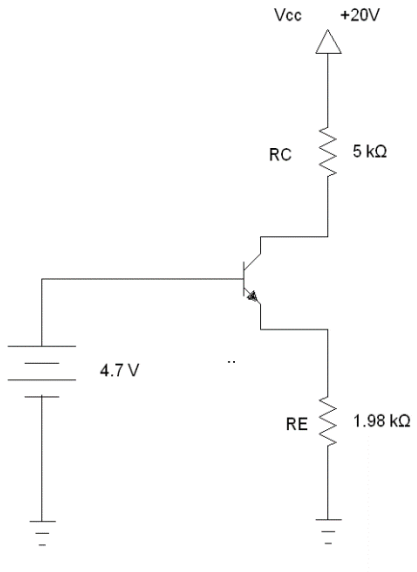
This amplifier is inverting. Note that the gain is in part determined by the voltage divider comprised of R_B and r_π. Reducing R_B would increase the gain but this would cause the amplifier to saturate. An interesting and undesirable property of this amplifier configuration is its dependence upon the value of β. The value of β determines the collector current and as a result the values of r_π and g_m. The problem with a high dependence on β is that β is varies from transistor to transistor even of the same type. If you examine a typical NPN datasheet you will find a wide range of values given for β that depend upon tolerance, temperature, and collector current to name a few. As a consequence, engineers create amplifier circuit designs where performance is relatively independent upon the value of β. A way to reduce the dependence is to use emitter bias rather than base bias as the next example illustrates.

Example 28: Simple Amplifier with Emitter Bias

Determine the voltage gain for the amplifier below.



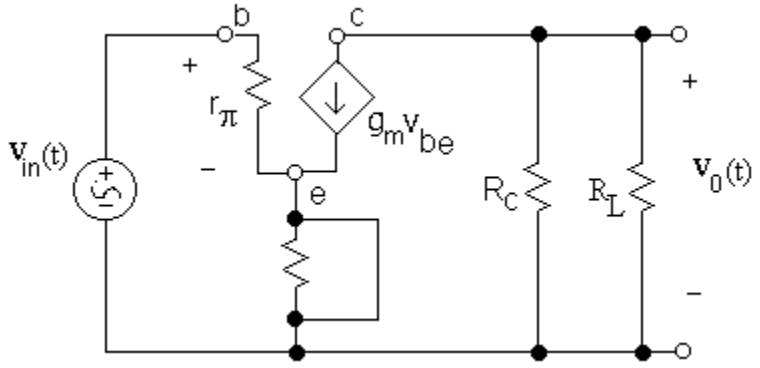
We begin by performing DC analysis in order to find I_{CQ}.



$$I_E = \frac{4.7 - 0.7}{1.98K} = 2.02\ mA$$
$$I_C = I_E \times \left(\frac{\beta}{\beta + 1}\right) = 2.00\ mA$$

The emitter resistor value and V_{BB} determine I_E. Note that I_C is not highly dependent upon the value of β; an advantage using emitter bias. In fact, if increase β from 100 to 200, I_C changes increases only 0.5%!

The value of I_C determined above is the same as the previous example and therefore the values for g_m and r_π are the same. The small signal equivalent circuit is shown below. If we assume that the coupling and bypass capacitors are large enough that their impedance is close to zero for the small signals of interest, we can replace them with short circuits and draw the circuit shown in the circuit below.



$$v_{out} = -g_m v_{be}(R_C // \mathrm{R_L})$$

Since $v_{be} = v_{in}$

$$A_V = -g_m(R_C // \mathrm{R_L})$$

Substituting the parameter values yields:

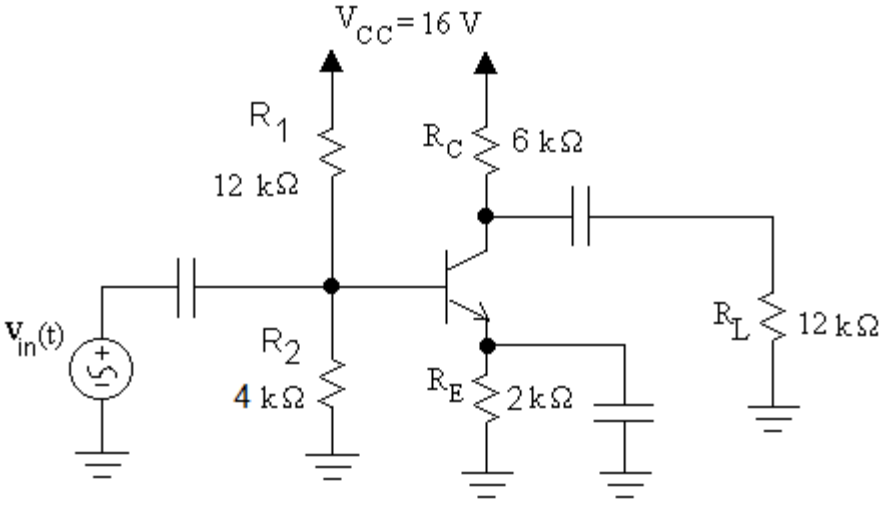
$$A_V = (-0.077)(2.5\ K)$$

$$A_V = -193\ V/V$$

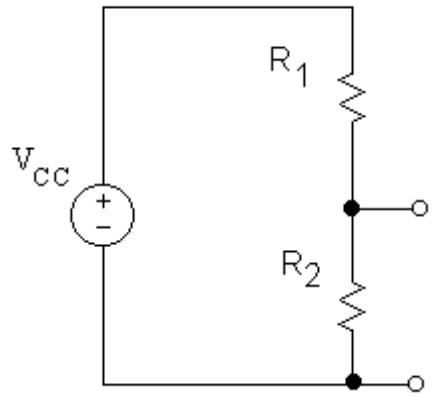
The previous examples were somewhat impractical amplifier circuits in that they required 2 power supplies. A more typical BJT amplifier circuit uses a single power supply along with a 4-resistor bias network as we illustrate in the next example.

Example 29: Example common emitter amplifier with 4-resistor bias network.

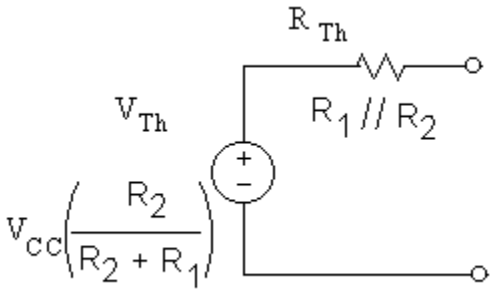
The circuit below represents a "common emitter" amplifier so named because the emitter terminal is common to both the input side and output side of the transistor. The previous examples also had the common emitter configuration.



We begin by performing a DC analysis to determine I_{CQ} which will allow us to find the small signal parameters. The resistors R_1 and R_2 form an "almost" voltage divider. It's not a true voltage divider because the resistors are not in series as a small amount of current flows into the base of the transistor. Although we cannot use voltage division without a loss of accuracy, we can simplify the left side of the circuit (shown below) by determining its Thevenin Equivalent.

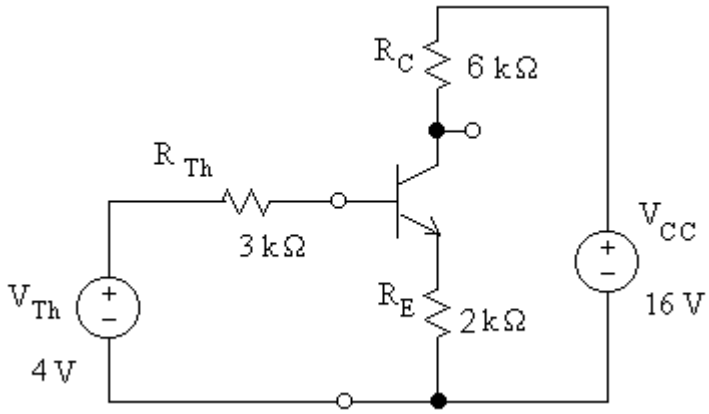


Left Side of Bias Circuit



Thevenin Equivalent

Replacing the left side of the circuit with its Thevenin equivalent and inserting in the original circuit yields the circuit below.



We assume the transistor is operating in the active region. Using KVL we write.

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

We next substitute $I_E = (\beta + 1) I_B$ into this equation and solve for I_B which yields:

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

$$I_B = \frac{4 - 0.7}{3\text{k} + (100 + 1)2\text{k}} = 16.1\ \mu A$$

$$I_C = \beta I_B = 1.61\ \text{mA}$$

$$I_E = I_B + I_C = 1.63\ \text{mA}$$

Next we calculate the terminal voltages to determine if the transistor is in the active mode.

$$V_C = V_{CC} - I_C \times R_C = (16) - (1.61\text{m})(6\text{k}) = 6.34\ \text{V}$$

$$V_E = I_E \times R_E = (1.63)(2\text{k}) = 3.26\ V$$

Now that we have the terminal voltages, we can check the active mode assumption.

$$V_{CE} = V_C - V_E = 6.34 - 3.26 = 3.08\ V$$

$$I_B > 0 \quad \surd$$

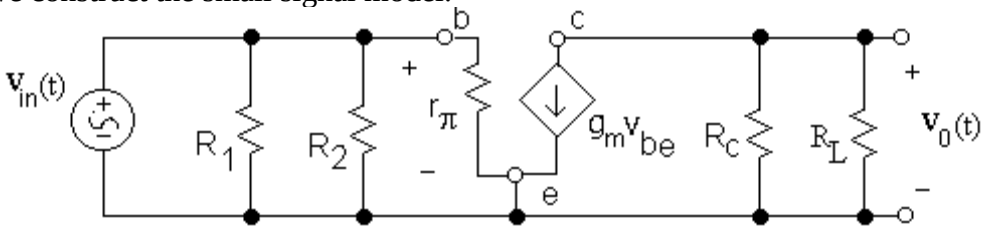
$$V_{CE} > 0.2\ V \quad \surd$$

The transistor is indeed operating in the active mode. The next step is to perform the small signal analysis. In order to do so, we calculate the small signal parameters g_m and r_π and construct the small signal model of the circuit.

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.61m}{25m} = 64.4\ \text{m}A/V$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 25m}{1.61m} = 1552\ \Omega$$

Next we construct the small signal model.



To calculate the voltage gain we find that the output voltage is:

$$v_{out} = -g_m v_{be}(R_C // \text{R}_\text{L})$$

Note that $v_{be} = v_{in}$. Therefore:

$$A_V = -g_m(R_C // \text{R}_\text{L})$$

$$A_V = -64.4\text{m}(6\ \text{k} // 12\ \text{k})$$

$$A_V = -257\ V/V$$

The Voltage Amplifier Model and BJTs

From our discussion of MOSFETs, you may remember the voltage amplifier model shown below.

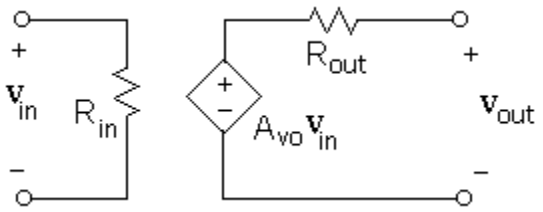


Figure 108: Voltage Amplifier Model

The analysis of BJT amplifiers can be simplified using this model. To illustrate, we shall determine the voltage amplifier model of the common emitter amplifier with a 4 resistor bias network that was examined in the previous example and reproduced below.

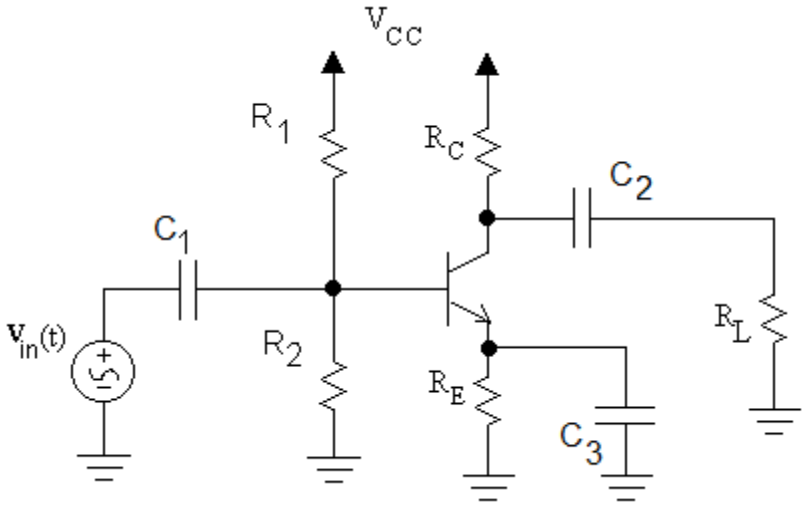


Figure 109: Common Emitter Amplifier Circuit

The small signal model for this circuit is shown in Figure 110 below along with the input and output resistance terminals. Our goal is to determine the voltage amplifier model for the circuit between the R_{in} and R_{out} terminals. We begin by determining R_{in}.

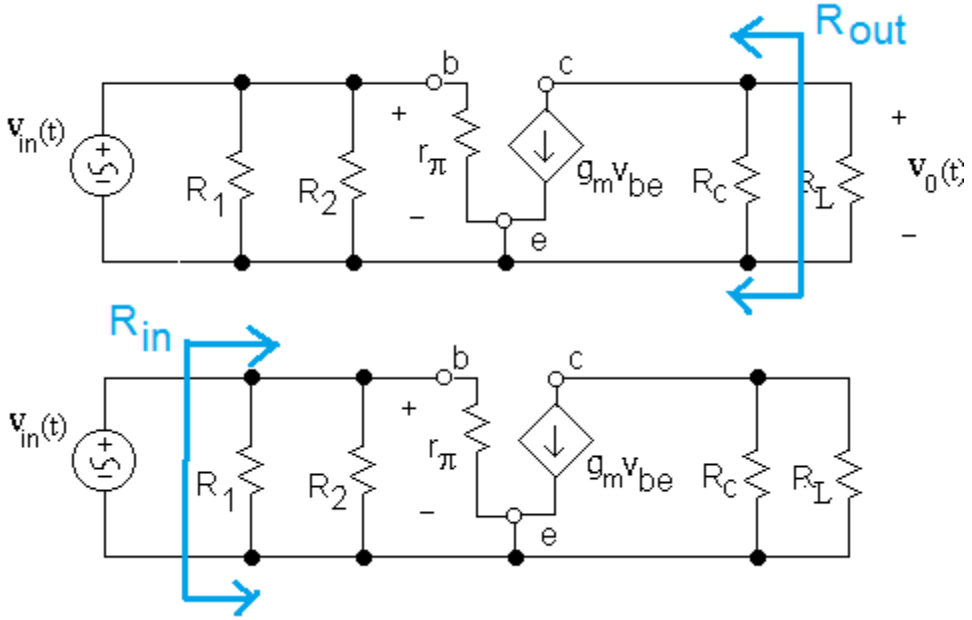


Figure 110: R_{in} and R_{out} Parameters for Common Emitter Amplifier

R_{in} is the resistance seen looking into the input terminals of the amplifier. In this case we can determine by inspection R_{in}.

$$R_{in} = R_1 // R_2 // r_\pi$$

R_{out} is the resistance at the output of the amplifier. To find R_{out}, we set the signal source to zero and apply a test voltage and determine the resulting test current. The output resistance is:

$$R_{out} = \frac{v_{test}}{i_{test}}$$

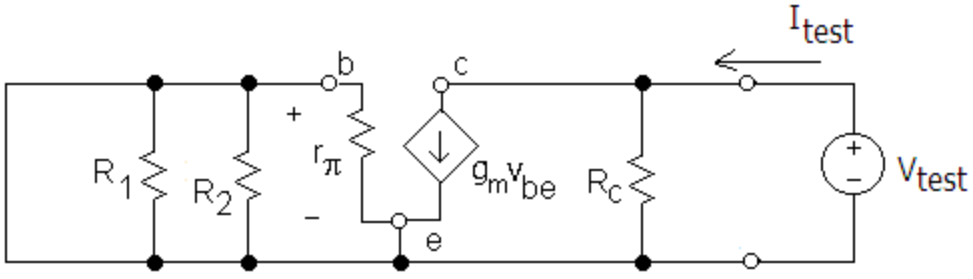


Figure 111: Determining R_{out}

Using KCL at the top right node yields:

$$g_m v_{be} + \frac{V_{test}}{R_C} - I_{test} = 0$$

Note that v_{be}=0 because of the short circuit at the input terminals. Therefore:

$$I_{test} = \frac{V_{test}}{R_C}$$

This yields:

$$R_{out} = \frac{V_{test}}{I_{test}} = \frac{V_{test}}{\frac{V_{test}}{R_C}} = R_C$$

We could shorten the analysis by simply noting that the dependent current source can be replaced by an open circuit because $v_{be}=0$ and tell by inspection that $R_{out}=R_C$. Not shown in this derivation but yet quite important is the fact that for the common emitter amplifier, the values of R_{in} and R_{out} are independent of R_S (if present) and R_L (if present).

Next we calculate A_{VO}, the voltage gain with the load removed.

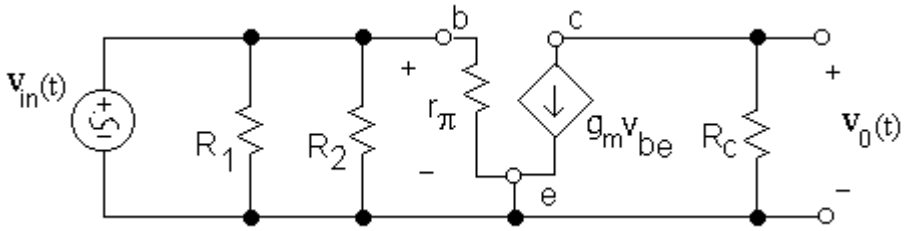


Figure 112: Determining A_V

By inspection we see that $v_o=- g_m v_{be} R_C$. We note that $v_{be}=v_{in}$ so the open circuit gain is:

$$A_{vo} = \left.\frac{v_o}{v_{in}}\right|_{R_L=\infty} = -g_m R_C$$

Now that R_{in}, R_{out}, and A_{VO} have been determined, we can construct the voltage amplifier model for the common emitter amplifier as shown in Figure 113.

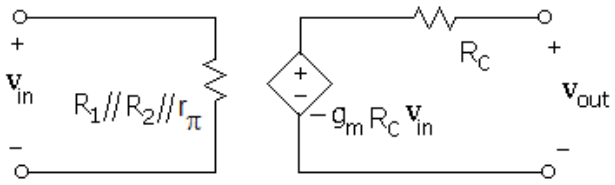


Figure 113: Voltage Amplifier Model of Common Emitter Amplifier

We can use this model to determine the voltage gain (or other parameters of interest) of a common emitter amplifier that has a load and/or practical source attached to it. For instance, let's find the voltage gain of the following circuit.

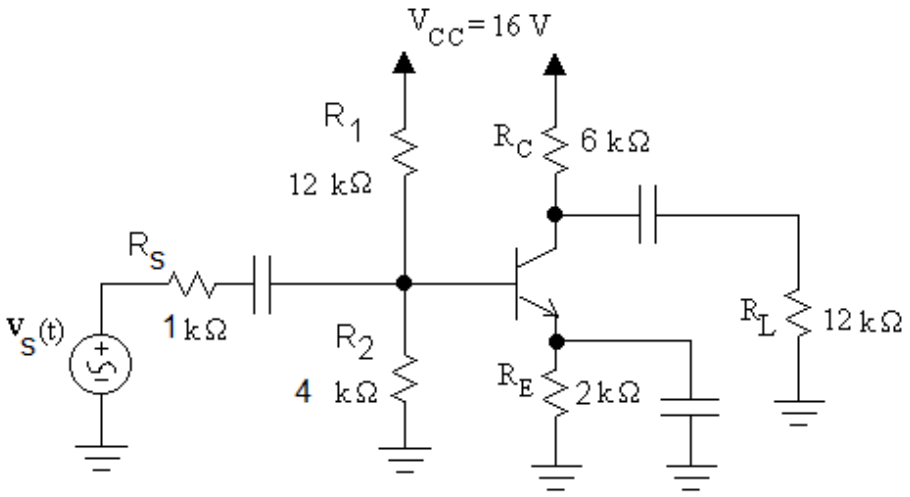


Figure 114: Common Emitter Amplifier with Circuit Parameter Values

This is the same circuit as that examined in Example 29 with the exception that a source resistance has been added. Our goal is to determine the voltage amplifier model and use the model to determine the voltage gain ($A_v=v_{out}/v_s$) of the circuit.

Using the previous results we can replace the small signal model with the voltage amplifier model and terminate the model with the given source and load.

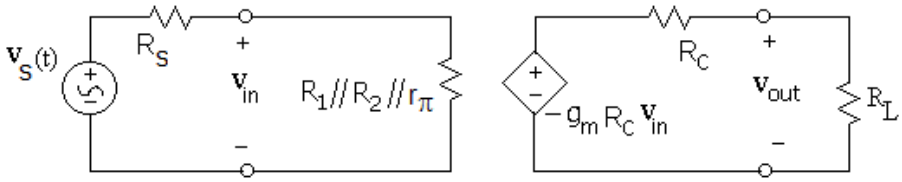


Figure 115: Terminated Voltage Amplifier Model of Common Emitter Amplifier

To determine gain we find that:

$$v_{in} = v_s\left(\frac{R_1//R_2//r_\pi}{R_s + R_1//R_2//r_\pi}\right)$$
$$v_{out} = -g_m R_C v_{in}\left(\frac{R_L}{R_L + R_C}\right)$$

Solving yields:

$$A_V = \frac{v_{out}}{v_s} = -g_m R_C\left(\frac{R_1//R_2//r_\pi}{R_s + R_1//R_2//r_\pi}\right)\left(\frac{R_L}{R_L + R_C}\right)$$

Note that if R_S =0, this equation would simplify to $A_V = -g_m(R_C//R_L)$ which should be of some comfort as this confirms the result we found in Example 29

Substituting the parameter values yields:

$$A_V = -(64.4\text{m})(6k)\left(\frac{12k//4k//1552}{1k + 12k//4k//1552}\right)\left(\frac{12k}{12k + 6k}\right)$$

$$A_V = -127\ V/V$$

Compared to the previous example, the gain of the circuit has been reduced because of the added source resistance. If the input resistance to the amplifier was infinite, we would get the same result as the previous example. This illustrates why it is desirable to have a high input resistance so that the gain of the amplifier is not negatively impacted by the internal resistance of the attached source. Similarly, the gain of the circuit increases as the output resistance of the amplifier decreases. However, in the common emitter amplifier circuit that we just analyzed, reducing the output resistance involves reducing R_C which will reduce A_{VO}.

List of Examples

List of Figures

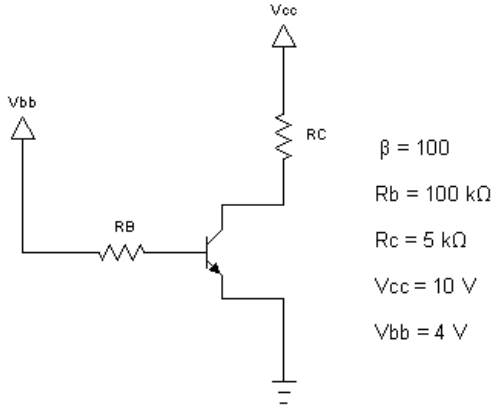
Problems

1. Find the operating region of NPN transistors with the following terminal voltages:
   a. V_B=2 V, V_E=1.3 V, V_C =2 V.
   b. V_B=4 V, V_E=3.3 V, V_C =3.5 V.
   c. V_B=4 V, V_E=3.7 V, V_C =6.2 V.

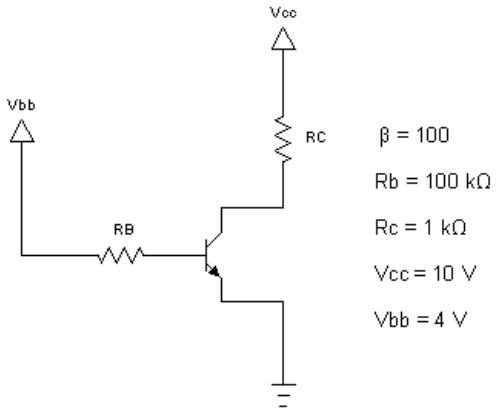
2. An NPN transistor has V_B=4 V and V_E=3.3 V. For what values of V_C will the transistor be operating in the active region?

3. An NPN Transistor has the following terminal voltages and currents: V_C=6V, V_E=4 V, and I_B=10μA. Find I_C, I_E, and V_B. Assume β=100.

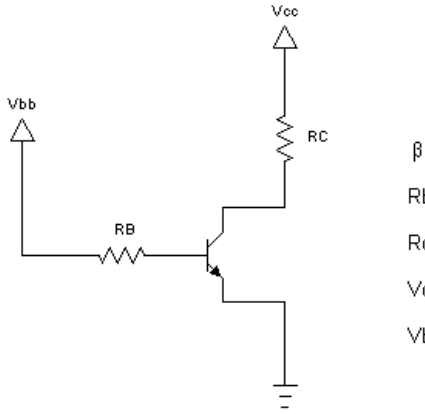
4. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below.



5. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below.

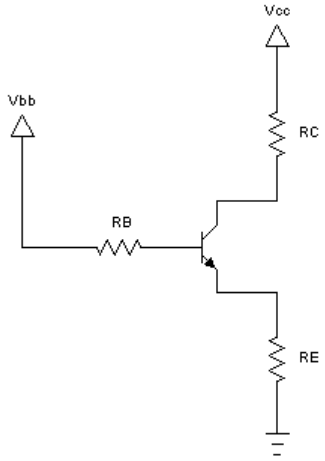


6. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below.



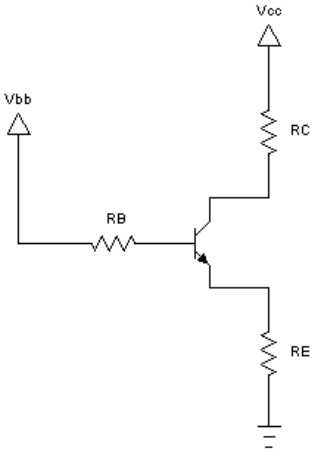
β = 100
Rb = 100 kΩ
Rc = 5 kΩ
Vcc = 10 V
Vbb = 2.7 V

7. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below.



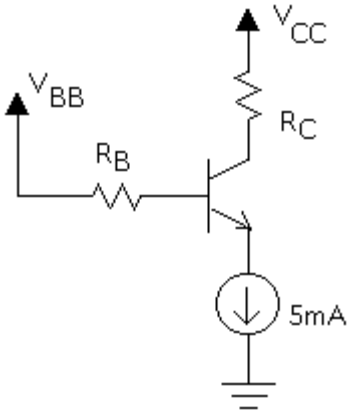
β = 100
Rb = 100 kΩ
Rc = 1 kΩ
Vcc = 10 V
Vbb = 3.7 V
Re = 1 kΩ

8. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below. Note that the value of β is 1000!

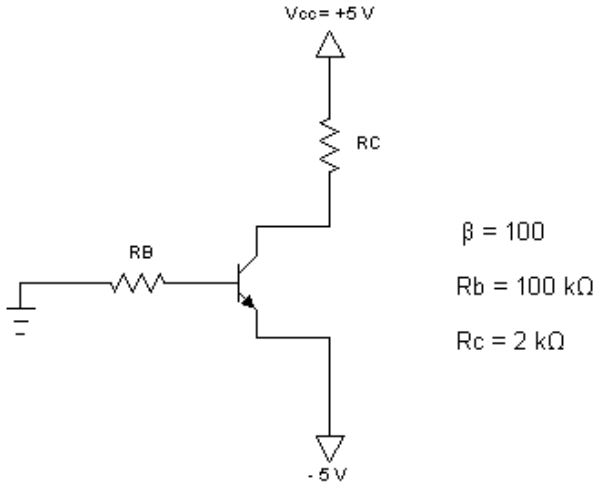


β = 1000
Rb = 100 kΩ
Rc = 1 kΩ
Vcc = 10 V
Vbb = 3.7 V
Re = 1 kΩ

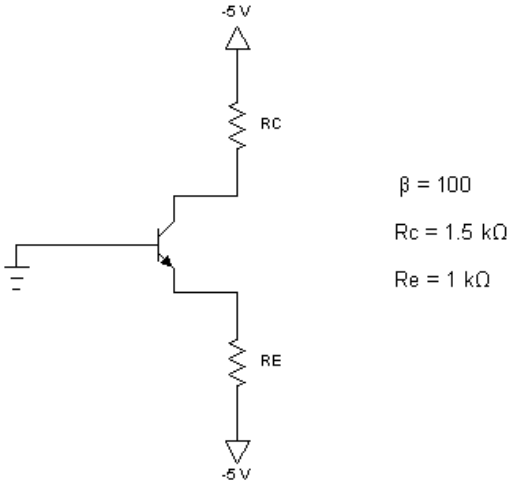
9. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below. Assume V_{CC}=10 V, V_{BB}=10 V, R_B=100 kΩ, R_C=500 Ω, and β=100.



10. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below.

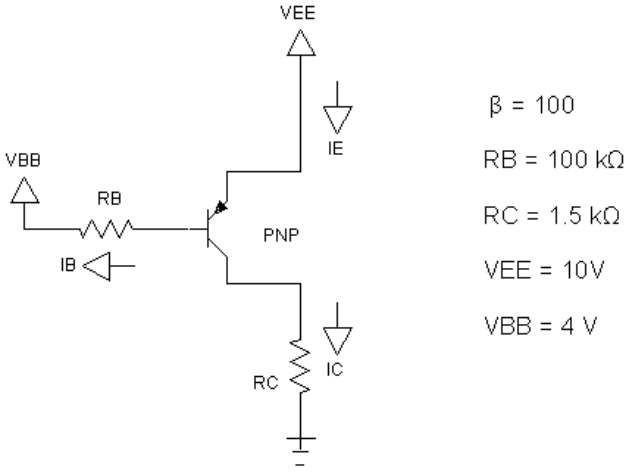


11. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit below.

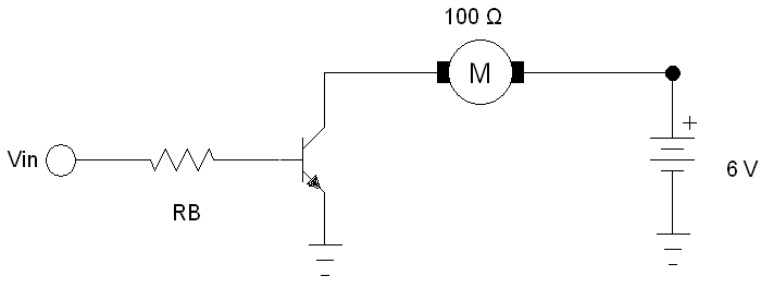


12. Find the operating region of a PNP transistor with the following terminal voltages:
    a. V_B=2 V, V_E=2.7 V, V_C =1 V.
    b. V_B=3.3 V, V_E=4 V, V_C =2 V.
    c. V_B=3.3 V, V_E=4 V, V_C =3.8 V
    d. V_B=4 V, V_E=3.7 V, V_C =2 V.
    e. V_B=2 V, V_E=1.3 V, V_C =1 V.

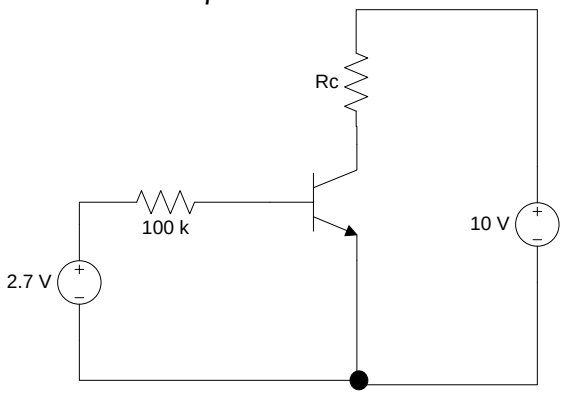
13. Determine all transistor terminal voltages (V_B, V_C, and V_E) and currents (I_B, I_C, and I_E) for the circuit PNP transistor below.



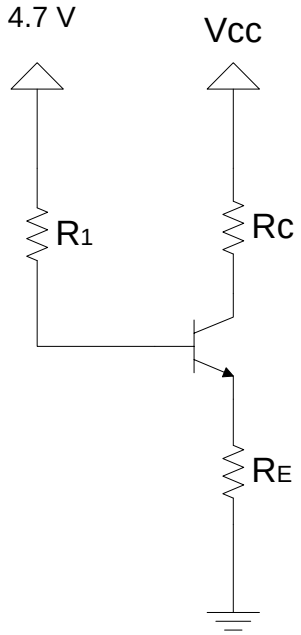
14. Design a motor driver circuit using an NPN transistor and an overdrive factor of 3. Assume that the voltage V_{in} = 0 or 5 V. Assume β=100 and that R_{motor}=100 **Ω**.



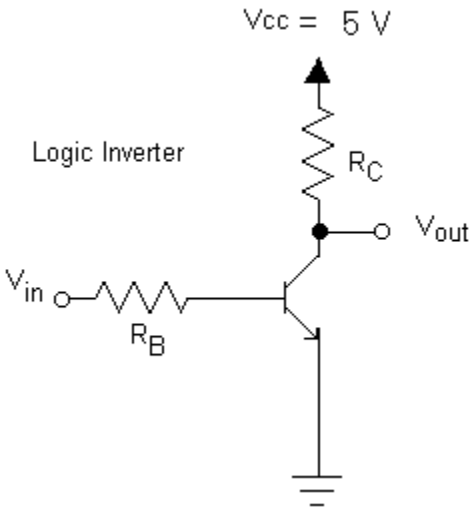
15. What is the largest value of R_C for the circuit below to remain in the active mode. Assume β=100.



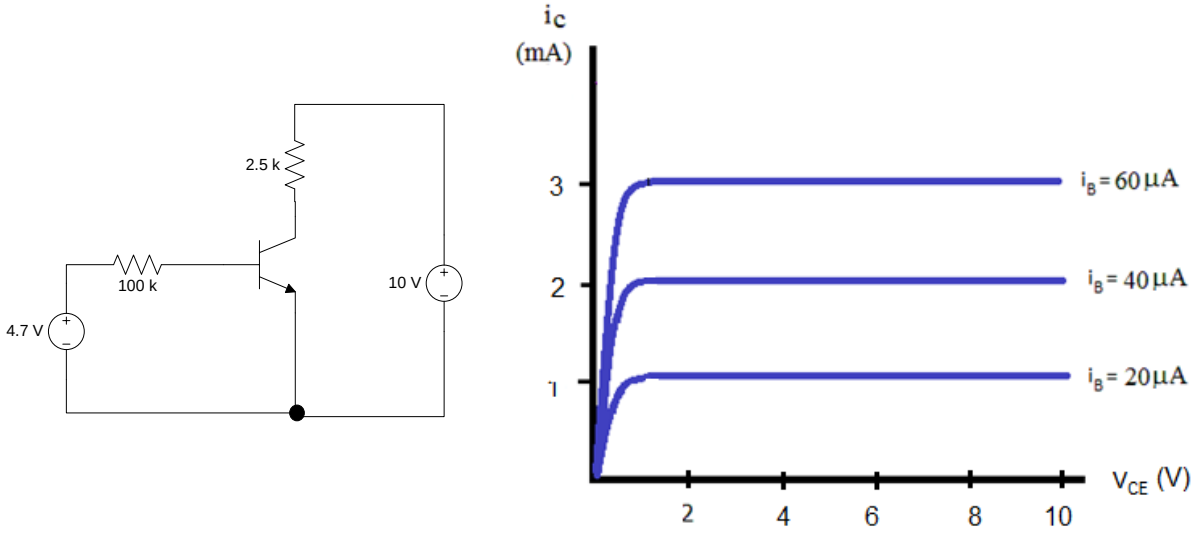
16. Find range of values of V_{CC} will result in saturation for the circuit below. Assume that R_1=40 kΩ, R_C=4 kΩ, R_E=1 kΩ, and β=100.



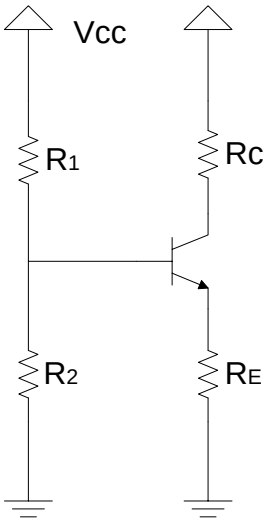
17. Draw the transfer characteristic graph showing v_{out} vs v_{in} for the inverter circuit below for V_{in} from 0 to 5 V. Drawing a single graph, include plots for R_C=2 kΩ, 10 kΩ, and 50 kΩ. Assume β=100 and R_B=100 kΩ. Judging from your graph, do any of these values for R_C seem unreasonable for a logic inverter?



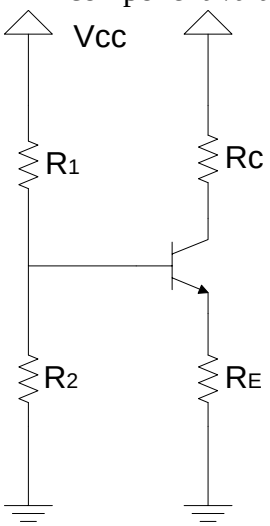
18. Determine V_C for the circuit below. Use the constant voltage drop model to find i_B. Then use load line analysis to find i_C.



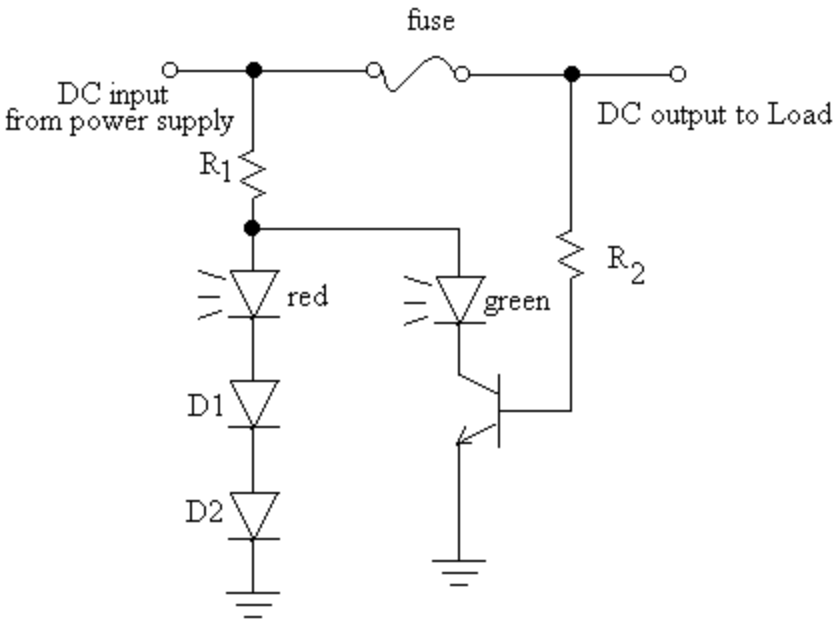
19. Determine all terminal voltages and currents for the circuit below. Assume the following component values: V_{CC}=20 V, R_1=400 kΩ, R_2= 600 kΩ, R_C=4 kΩ, R_E=0, and β=100.



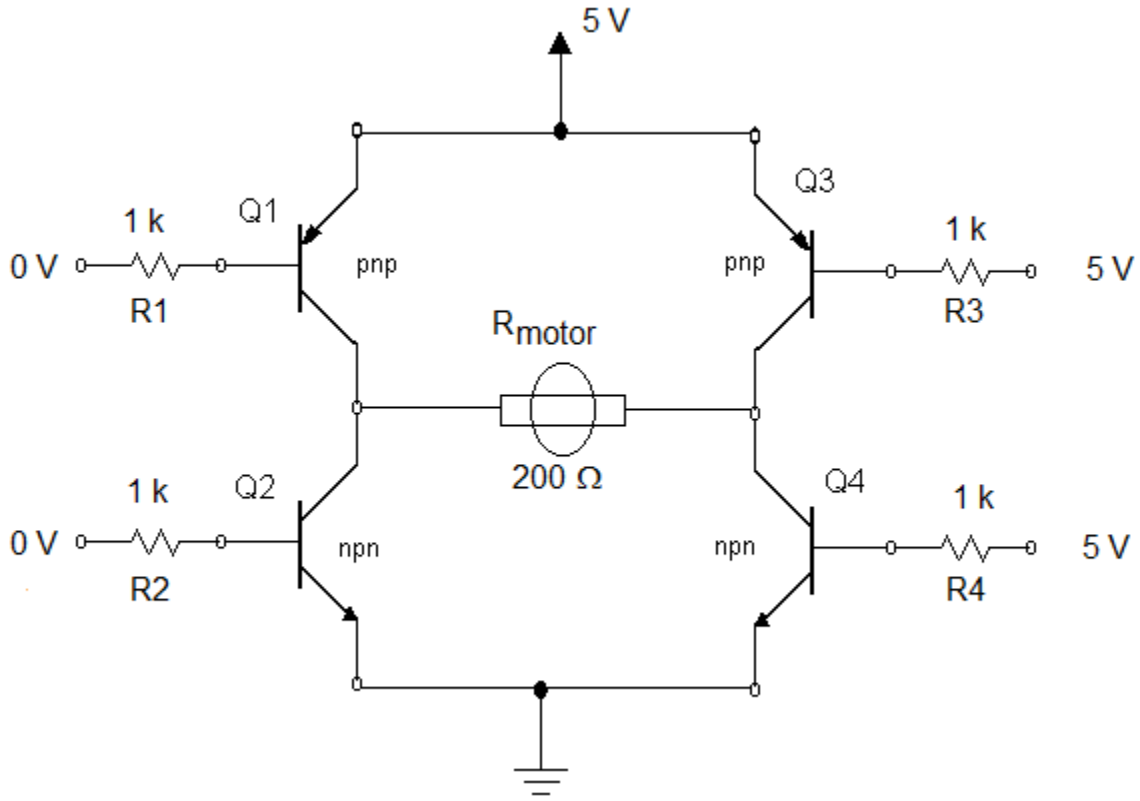
20. Determine all terminal voltages and currents for the circuit below. Assume the following component values: V_{CC}=20 V, R_1=40 kΩ, R_2= 60 kΩ, R_C=1 kΩ, R_E=1 kΩ, and β=100.



21. Design an LED driver circuit that will supply 60 mA of current to a string of LEDs. Assume that the β of the NPN transistor varies between 100 and 200 depending on temperature. Assume that the supply voltage is 10 V. (Hint: because of the variability of β, use an emitter resistor to make the circuit less dependent upon β). Assume that a voltage V_{in} is attached to the base of the transistor and that V_{in} = 5 V is used to turn on the LED and 0 V turns it off. Use R_B=0 and select an appropriate R_E.
22. ~~Create an LED driver circuit using an NPN transistor that will supply either 30 or 60 mA depending upon the position of a SPST switch.~~
23. A blown fuse indicator circuit is shown below. When the fuse is intact, the green LED is on and the red LED off. When the fuse is blown, the red LED is on and the green off. Clearly explain how this circuit works. Assume that the green and red LED forward voltage drops are both 2 V and the junction diode forward drops are 0.7 V. Also assume that R2 has been selected so that the transistor is in the saturation mode when the fuse is intact.



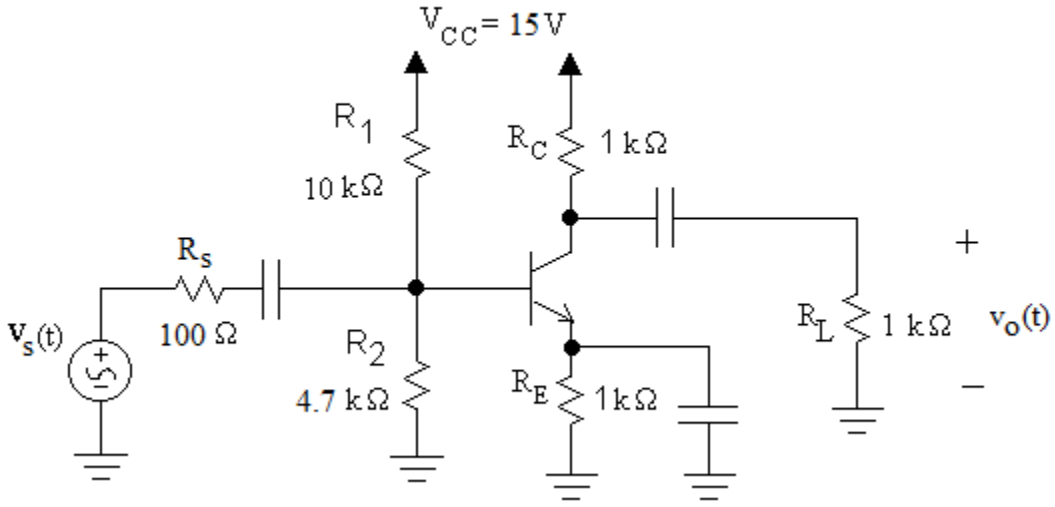
24. If the DC input voltage from the power supply is 5 V, select R1 and R2 so that the current flow through the LEDs is limited to approximately 20 mA. A current of 5 mA is sufficient to turn on either LED. Assume β=200.
25. Determine the voltage drop across the motor and the base current for Q1 and Q4. Assume that transistors are biased such that they are either in cutoff or saturation.



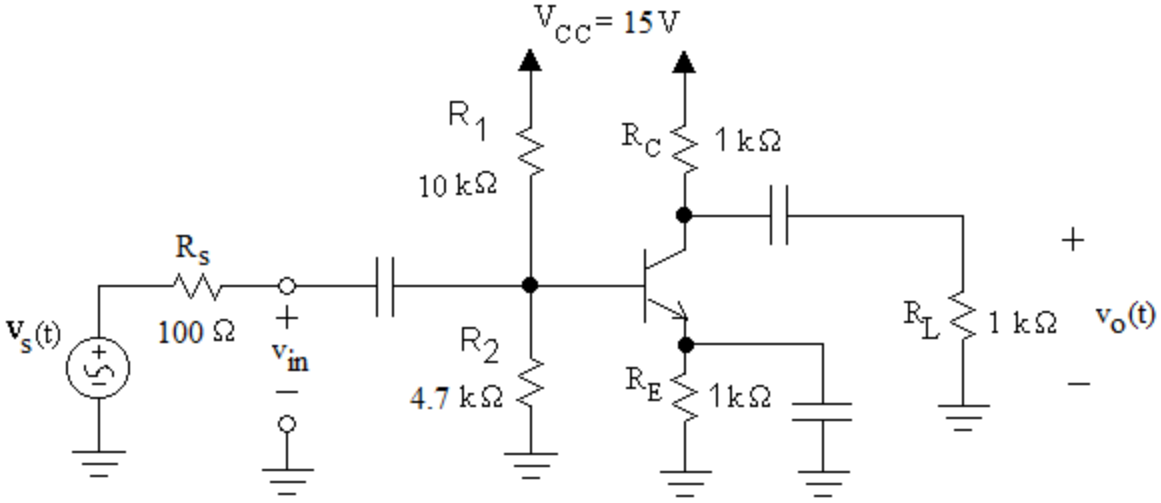
26. Run the current mirror simulation in the Java circuit simulator. Explain how the current mirror works.

27. Design a current mirror current source using NPN transistors that produces 20 mA of current. Assume the load resistance ranges from 100 ohms to 300 ohms. In your design, specify the minimum voltage source that can applied to the load.

28. Determine the voltage gain A_v of the circuit below. Assume β =100 and V_T =25 mV.

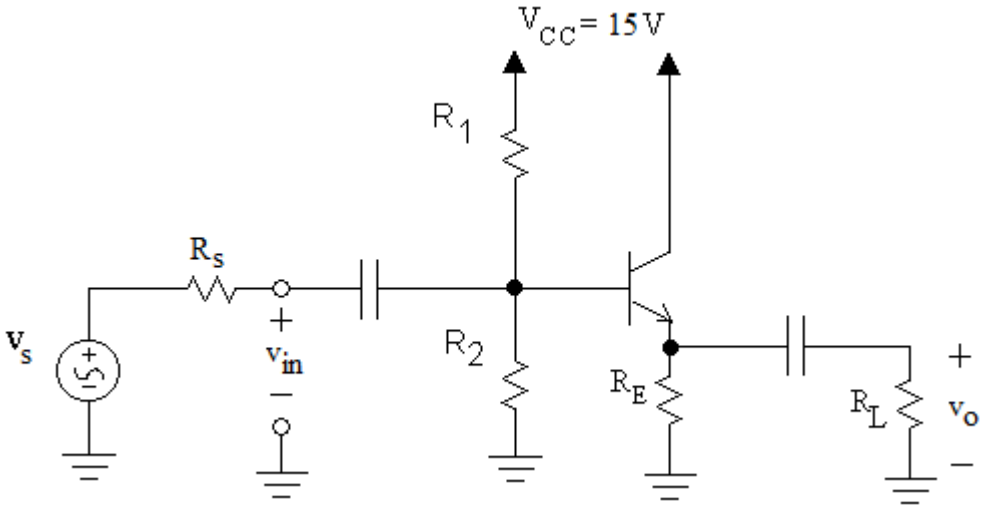


29. Determine A_{vo}, R_{in}, R_o for the amplifier below. Draw the voltage amplifier model for this circuit. Assume β =100 and V_T =25 mV.

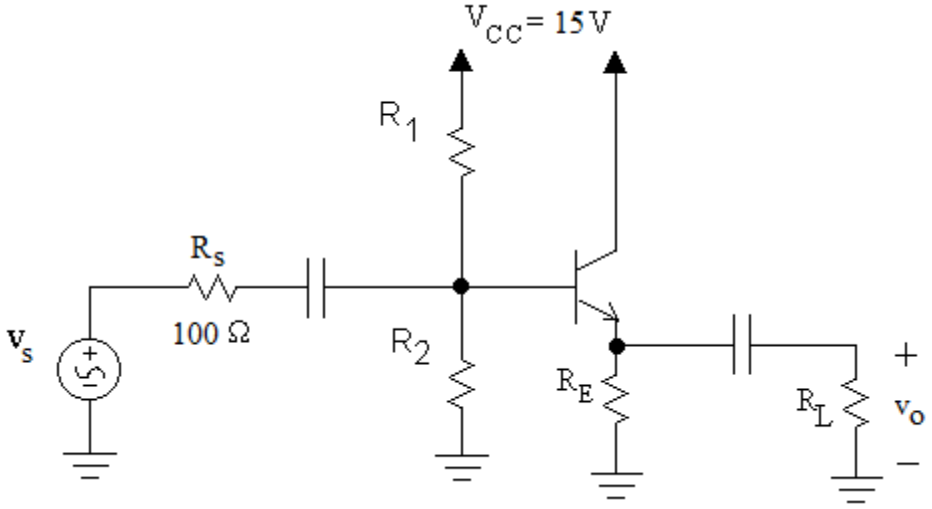


30. Using voltage amplifier model you determined in problem 29, determine A_v and A_i for this circuit with the source and load resistors shown.

31. The circuit below is knows as an emitter follower amplifier. Determine its voltage amplifier model for this amplifier in terms of r_π, g_m, R_1, R_2, R_S, R_L, and R_E. Assume the amplifier is operating in the active region. Note that unlike the common emitter amplifier, The values for R_{in} and R_{out} are dependent upon R_L and R_S respectively.



32. Determine A_v and A_i for the emitter follower amplifier shown below. Assume that β=100, V_T =25 mV, R_1=R_2=5kΩ and R_E=R_L=1kΩ. If you have done problem 31, you can use those results to help solve this problem.



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