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Novel high-performance QCA Fredkin gate and designing scalable QCA binary to gray and vice versa

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Abstract

In the design of digital logic circuits, QCA technology is an excellent alternative to CMOS technology. Its advantages over CMOS include low power consumption, fast circuit switching, and nanoscale design. Circuits that convert data between different formats are code converters. Code converters have an essential role in high-performance computing and signal processing. In this paper, first, we proposed a novel QCA structure for the quantum reversible Fredkin gate. Second, we proposed 4-bit and 8-bit QCA binary-to-gray converter and vice versa. For the second proposal, both reversible and irreversible structures are suggested. The proposed structures are scalable up to N bits. To change the conversion type from B2G to G2B, we use a 2:1 QCA multiplexer. The proposed QCA Fredkin is applied in the reversible design of QCA code converters as multiplexers. The suggested designs are simulated using the QCADesigner tool. Then we calculated figures of merit, including cell counts, occupied areas, and clock zones. Finally, we compare the proposed structures to existing research. Our proposed approach is the first quantum-dot cellular automata design to perform B2G conversion and G2B in a single QCA circuit. The proposed designs are scalable. Specifications are reported.

Keywords Quantum computing (QC) · Quantum-dot cellular automata (QCA) · Fredkin gate (FRG) · Binary to gray (B2G) · Gray to binary (G2B) · Scalable design · Parity-preserving reversible gate · Conservative gate

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1 Introduction

The CMOS technology faces challenges like leakage current, speed limitation, and power consumption. Landauer demonstrated that non-reversible processing of the information leads to energy losses due to data loss [1, 37, 38]. Researchers have considered different technologies to overcome the limitations of CMOS technology and reduce the loss of energy. They found QCA one of the most appropriate substitutions for CMOS technology [2]. The QCA technology has advantages such as low power consumption, fast switching, and the capability to design circuits on the nanoscale [3]. QCA technology employs in the design of reversible logic gates. Gates are reversible if their outputs produce their inputs and vice versa. Reversible logic gates eliminate any information loss. There is no energy loss in a circuit that has no information loss.

A code converter generally turns data from one format to another. Signal processing depends heavily on code converters. In a binary-to-gray (B2G) code converter, binary numbers are input and converted into gray codes following processing. The gray-to-binary (G2B) code converter takes numbers in gray form as inputs and converts them into binary codes after processing. During the past few years, circuits like fault-tolerance B2G [4], binary incrementer [5], reversible ALU [6], hamming code circuit [7], reversible full adder [8], and multiplier [9] have been designed in QCA. A 3-bit B2G conversion and vice versa in the reversible and irreversible modes is proposed in [10]. Gray codes are beneficial when a binary number transition results in an error or ambiguity. As a result, since only one bit changes during a transition from one number to another, gray code will efficiently handle this problem. Other gray code applications are Boolean circuit minimization, genetic algorithms, mathematical puzzles, and position encoders. Some of the contributions and highlights of this paper are as follows:

- Designing and simulating a 4-bit irreversible B2G conversion and vice versa in QCA technology
- Designing and simulating an 8-bit irreversible B2G conversion and vice versa in QCA technology
- Designing and simulating an N-bit irreversible B2G conversion and vice versa in QCA technology
- Proposing and simulating a novel structure of reversible Fredkin (FRG) gate in QCA technology
- Designing and simulating a 4-bit reversible B2G conversion and vice versa in QCA technology
- Designing and simulating an 8-bit reversible B2G conversion and vice versa in QCA technology
- Designing and simulating an N-bit reversible B2G conversion and vice versa in QCA technology
- Verifying the designs using QCADesigner [11]
- Power dissipation analysis of the proposed irreversible and reversible B2G and vice versa

- Comparing the designs with recent works regarding different figures of merit, including the cell counts, the occupied area, and the latency.
- Our proposed approach is the first design to embed both B2G and G2B in QCA technology in a single circuit.

The organization of the rest of the paper is as follows: In Sect. 2, we provide the fundamentals of QCA technology. In Sect. 3, the previous works are discussed. The proposed QCA structures of Fredkin gate and code converters and their simulations are fully described in Sect. 4. Evaluation parameters for the proposed N-bit code converter are also calculated in Sect. 4. Section 5 shows the simulation results of the suggested QCA designs using the QCADesigner tool. In Sect. 6, the suggested structures are compared to related research, and an energy dissipation analysis of the proposed structures are presented. In Sect. 7, we concluded our work and proposed some future research directions.

2 Fundamentals of QCA

For the paper to be self-contained, in this section, we briefly describe various aspects of QCA technology, including QCA cells, QCA wires, QCA majority, QCA inverters, and QCA clocks.

2.1 QCA cell

The QCA cells are the most basic blocks of quantum-dot cellular automata circuits. As shown in Fig. 1, each QCA cell has four quantum dots and two free electrons at every corner. Tunnel junctions separate the dots so that electrons can reposition from one location to another [12]. A QCA cell can take several states depending on the occupation of electrons inside the dots. The operation of the QCA relies on Coulombic interactions. Electrons remain diagonally oriented due to Coulombic interactions, as seen in Fig. 1a and b [13]. This causes two states of polarization to emerge, logic '0' ($P=-1$) and logic '1' ($P=+1$). P is the polarization of the cell [14]. Coulombic interactions enable neighboring QCA cells to exchange information; the state of one influences the state of the other.

2.2 QCA wire

In the design of logic circuits, designers use normal cells (in four zones), rotating cells, cells with fixed polarization, and input/output cells in QCA, as depicted in

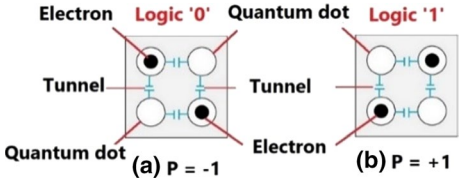


Fig.1 QCA cell Polarization [13] **a** Logic '0' **b** Logic '1'

Fig. 2 [8]. A binary wire is a set of cells horizontally or vertically that transmits information.

A QCA wire is formed by connecting several cells at 90°, as shown in Fig. 3a, or 45° side by side, as shown in Fig. 3b [15]. The signal propagates along the wire from left to right as the leftmost cells are activated. A line of QCA cells forms a 90-degree QCA wire. A QCA wire with 45° cells transfers the incoming signal into odd cells and inverts it into even cells. QCA technology has two types of wire-crossings: coplanar and multilayer. It is possible to perform a wire-crossing in one layer called a coplanar wire-crossing. Figure 4b shows a QCA wire with 45-degree cells crossing over a regular wire. Alternatively, wires on either side of the wire-crossing should have two-phase differences, as shown in Fig. 4a. According to Fig. 4c, multilayer crossovers use multilayered architectures to pass the QCA wires over each other [16].

2.2.1 QCA clocking

Wires are divided into multiple clock zones to avoid signal degradation caused by a long chain of cells in the same clock zone. A QCA circuit uses the clock to synchronize

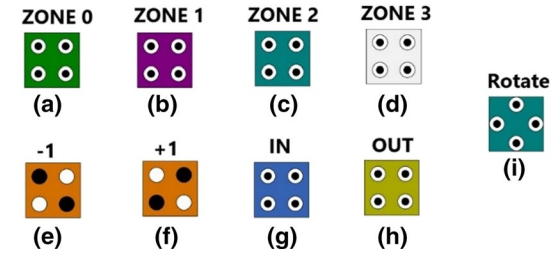


Fig. 2 QCA wire: **a**–**d** normal cells **e**–**f** fix polarization cells **g** input cell **h** output cell i) rotate cell

Fig. 3 The QCA wire [8] **a** 90° **b** 45°

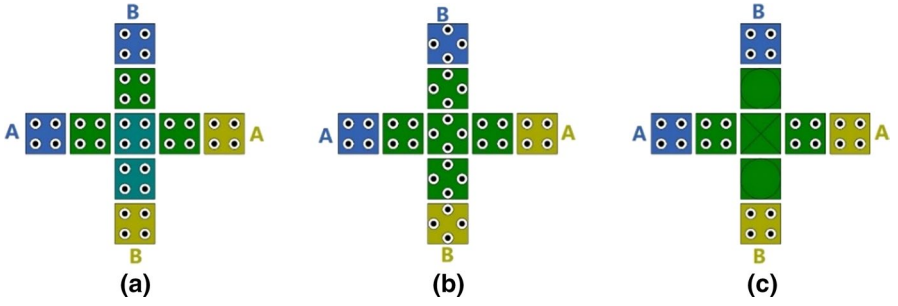


Fig. 4 Types of wire-crossing [16] **a** coplanar with different phases **b** coplanar with rotate cell **c**) multilayer

and regulate information flow. In very large scale integrated (VLSI) circuits, a signal controls the time, while in QCA, the clock controls the storage and removal of information within cells [17]. For altering time in the circuit, QCA calculations require a multi-phase clock [18]. A QCA clock comprises four phases: switch, hold, release, and relax [19]. The phases are 90 degrees apart. During the switch phase, the QCA cell begins the transition from unpolarized to a polarized state, and the barriers between the dots rise. In the hold phase, the barrier of the cell is at its maximum, electrons cannot tunnel through the dots, and the polarization of the cell does not change. The barrier is decreased in the release phase, allowing electrons to tunnel through the dots, and the cell's states become unpolarized. In the relaxation phase, the barrier stays reduced, and the cell is unpolarized. This clocking scheme splits a QCA array into four sub-arrays called clock zones. According to this method, a clock zone can complete its computation in four phases [6].

2.3 QCA majority and inverter gates

In QCA-based logic implementation, the majority (MV) and the inverter (INV) gates are essential. The MV gate is a function logic that includes three inputs and one output. Equation (1) displays its inputs and outputs. In Eq. (1), A, B, and C are inputs, and MV is the output.

$$\mathrm{MV}(A, B, C) = \mathrm{AB} + \mathrm{AC} + \mathrm{BC} \tag{1}$$

QCA designs require a majority gate. Typically, a majority gate requires five cells for implementation. The inputs of this block are in the top, bottom, and left positions of the QCA design. The device cell in the center propagates the results to the cell on the right as output. Figure 5a depicts the QCA structure of the MV. Whenever one of the inputs equals 1, the MV turns into an OR gate, as shown in Fig. 5c. Equation (2) denotes the logic function of an OR gate in QCA. Whenever one of the inputs equals 0, the MV turns into an AND gate, as shown in Fig. 5b. Equation (3) denotes the logic function of an AND gate in QCA.

$$\mathrm{MV}(A, B, 1) = A + B \tag{2}$$

$$\mathrm{MV}(A, B, 0) = \mathrm{AB} \tag{3}$$

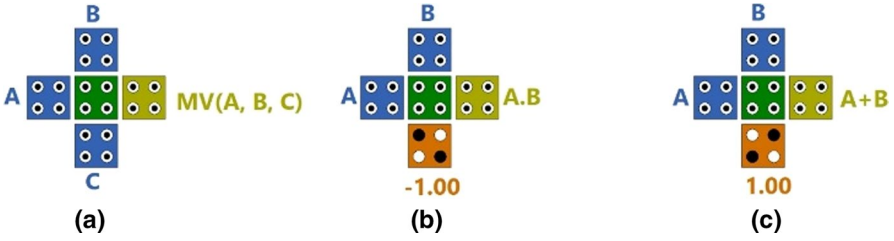


Fig. 5 Majority in QCA [20] **a** Structure **b** AND in QCA **c** OR in QCA

Inverter gates are another significant structure for implementing logical circuits using QCA. Cells aligned diagonally will have opposite polarizations. By aligning cells diagonally, an inverter can be created. Figure 6 shows two examples of inverters in different shapes.

3 Related works

This section reviews previous works on QCA code converters and QCA multiplexers. Xiao-bin et al. [22] introduced a 4-bit B2G code converter using 2-input XOR gates in QCA technology. They simulated their suggested design with the QCADesigner tool. The suggested code converter featured fewer cell counts, a smaller area, and decreased latency compared to prior studies. Rao et al. [23] proposed a B2G and a G2B code converter using their proposed XOR. The proposed XOR contains only 29 cells. It is much smaller than the previous design. The proposed design of the B2G code converter includes only 127 cells. The simulation result was compared and evaluated against recent research. Khakpour et al. [24] presented new structures for converting B2G, G2B, and BCD-to-gray codes in QCA. Also, they suggested a new structure for the XOR gate for the circuit. There are 76 QCA cells in the proposed G2B converter, and its delay is 2.25 cycles. The proposed B2G converter consists of 99 QCA cells with a delay of 0.75 cycles. Karkaj et al. [25] proposed a new structure of a 2-input XOR. Then, using it, they simulated reversible and irreversible B2G conversions. The proposed work has good improvements with cell counts and area occupied. The proposed circuit includes 92 cells and one crossover. Ahmed et al. [26] proposed efficient 4-bit, 8-bit, and 16-bit designs of separated B2G and G2B converters that can scale up to N bits. These converters utilize to design 4-bit, 8-bit, and 32-bit communication systems for sending and receiving data effectively. We use multiplexers to select a single path from multiple inputs. Jeon [27] presented a QCA multiplexer with 13 cells and then suggested a shift register based on the proposed multiplexer. Khan [28] presented a simple single-layer multiplexer without any wire-crossing. This 2:1 multiplexer is shown in Fig. 7.

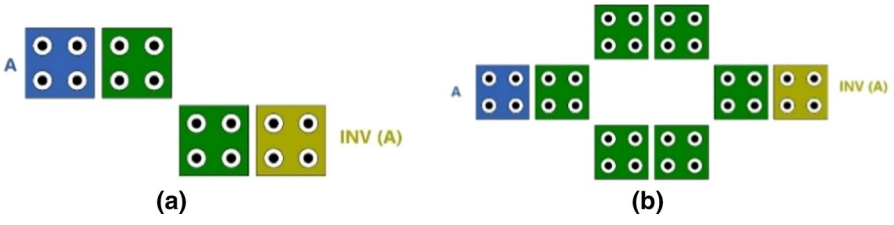


Fig. 6 Design of Inverter in QCA [21] **a** Simple Inverter. **b** Robust Inverter

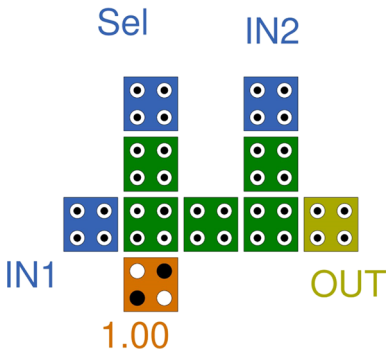


Fig. 7 The QCA 2:1 multiplexer in [28]

4 Proposed QCA structures

A code converter transforms one code into another code to perform signal processing. On the one hand, the B2G code converter takes inputs in a binary format and then processes them to produce a gray format. On the other hand, a G2B code converter accepts numbers in the gray format as inputs, processes them, and then outputs the binary form. We present a novel structure for the Fredkin gate in QCA technology to utilize in reversible designs. Also, we propose and simulate novel QCA B2G and G2B code converters. The designs are done using both reversible and non-reversible approaches for converting 4-, 8-, and N-bit codes. To cross wires in QCA circuits, designers employ coplanar and multilayer schemes. Because of the fabrication difficulties associated with multilayer crossover, designers utilize coplanar crossover for designing one-layer QCA circuits. Although more clocking zones are necessary for coplanar crossover, these zones address the problem of sneak noise paths. As a result, in this paper, we use the coplanar scheme to achieve robust designs based on QCAs. Also, we use the coherence vector simulation engine to check the accuracy of the proposed design [29]. Figure 8 shows the simulation parameters for verifying the results of the proposed QCA structures.

4.1 The Proposed reversible Fredkin gate

In this section, we propose a novel structure for the Fredkin gate in QCA technology. This gate has a quantum cost of five. It maps three inputs (‘*A*’, ‘*B*’, and ‘*C*’) to three outputs (‘*P*’, ‘*Q*’, and ‘*R*’). The values of ‘P’, ‘Q’, and ‘R’ are equal to $\mathbf{A}, \overline{\mathbf{A}}\mathbf{B} + \mathbf{AC}$, **and** $\mathbf{AB} + \overline{\mathbf{A}}\mathbf{C}$, respectively. The first input (i.e., ‘*A*’) acts as a control signal, while ‘B’ and ‘C’ represent data. The input ‘*A*’ is connected directly to the output ‘P’. If ‘$A = 0$, the outputs are identical to the inputs ($Q = $ B, and $R = $ C). Otherwise, if $A = 1$, the outputs correspond to the inputs swapped ($Q = $ C, $R = $ B). Fredkin gate is a conservative gate, i.e., it has equal number of 1 s in the outputs as there are in its inputs. Fredkin gate is also a parity-preserving gate, i.e., the input parity is equal to the output parity. Fredkin gate is important for both reversible and quantum computing. It has applications in designing parity-preserving reversible circuits. In

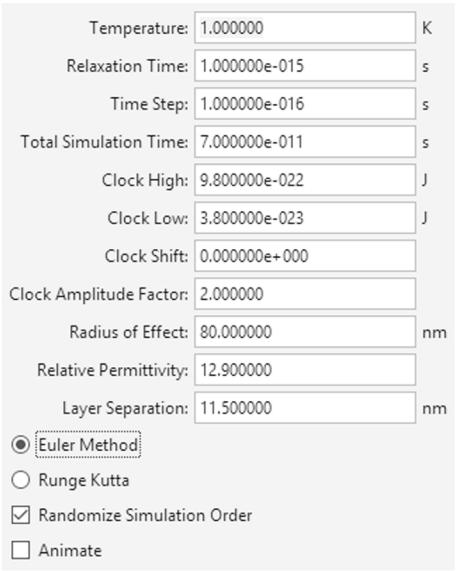


Fig. 8 The simulation parameters [29]

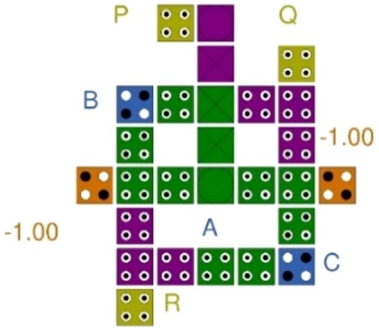
the block structure, Fredkin gate serves as the multiplexer. By this definition, this gate is responsible for converting binary into gray and vice versa. Figure 9 shows the QCA layout and the simulation result of the proposed reversible Fredkin gate. The structure contains 32 cells within an area of $0.025\mu m^2$, with a latency of two clock zones.

4.2 Proposed irreversible 4-bit B2G and vice versa

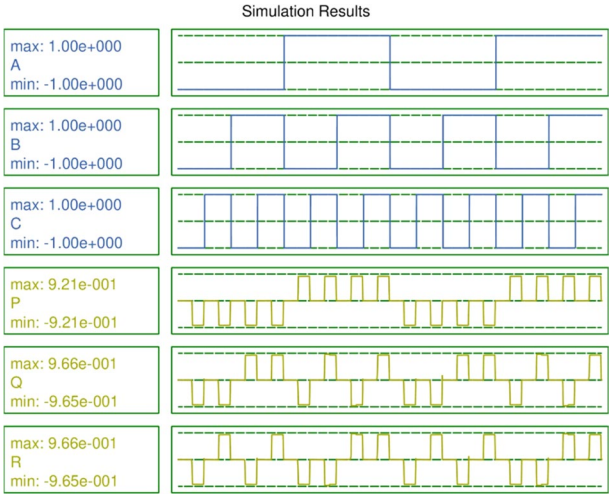
In this section, we design and simulate the non-reversible structure of a 4-bit B2G code converter and vice versa in QCA technology. A 4-bit B2G converts a 4-bit binary number into its gray equivalent. A 4-bit G2B conversion receives a 4-bit gray number as input and produces its binary equivalent in output. Figure 10 shows the logic circuit of the 4-bit B2G and vice versa. A_i, A_0 $and A_3$ are input, Least Significant Bit (LSB), and Most Significant Bit, respectively. SEL is a converter selector. The design uses three XOR gates and two multiplexers. Equation (4) shows the relationship between inputs and outputs.

$$\begin{cases} P_3 = A_3 \\ P_2 = A_3 \oplus A_2 \\ P_1 = A_1 \oplus \left(\overline{\text{SEL}}.A_2 \oplus \text{SEL}.\left(A_2 \oplus A_3\right)\right) \\ P_0 = A_0 \oplus \left(\overline{\text{SEL}}.A_1 \oplus \left(\text{SEL}.\left(A_1 \oplus A_2 \oplus A_3\right)\right)\right) \end{cases} \tag{4}$$

If SEL equals zero, the offered circuit operates as a B2G converter, and the equation becomes Eq. (5).



(a) Our proposed QCA Fredkin gate structure



(b) Simulation result

Fig. 9 The proposed QCA reversible Fredkin gate and its simulation result, **a** Our proposed QCA Fredkin gate structure, **b** Simulation result

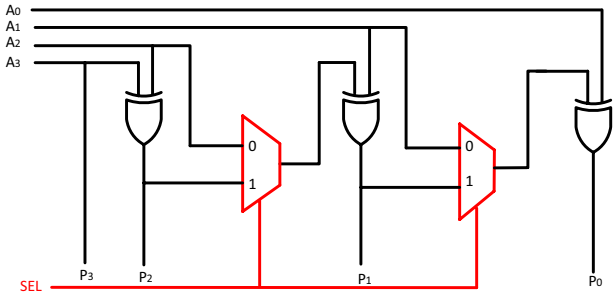


Fig. 10 The irreversible 4-bit B2G and vice versa

$$\text{If SEL} == 0 \Rightarrow \begin{cases} P_3 = A_3 \\ P_2 = A_3 \oplus A_2 \\ P_1 = A_2 \oplus A_1 \\ P_0 = A_1 \oplus A_0 \end{cases} \tag{5}$$

If SEL equals one, the offered circuit operates as a G2B converter, and the equation becomes Eq. (6).

$$\text{If SEL} == 1 \Rightarrow \begin{cases} P_3 = A_3 \\ P_2 = A_3 \oplus A_2 \\ P_1 = A_3 \oplus A_2 \oplus A_1 \\ P_0 = A_3 \oplus A_2 \oplus A_1 \oplus A_0 \end{cases} \tag{6}$$

Using Eqs. (5) and (6), one can understand the functionality of the B2G and G2B code converters. Table 1 is the truth table for the 4-bit B2G and G2B code converters.

Figure 11 shows the proposed design for the 4-bit B2G conversion in QCA technology. In this structure, A_i is the input vector and P_i is the output vector. The primary element of the suggested architecture consists of two-input XOR gates. Thus, we use the best XOR structure [21] in our simulations. This circuit includes 75 cells, an area of 0.08μm^2, and one clock cycle.

Table 1 Truth table for the 4-bit converter

Inputs (binary code) $A_3A_2A_1A_0$	B2G $P_3P_2P_1P_0$	G2B $P_3P_2P_1P_0$
0000	0000	0000
0001	0001	0001
0010	0011	0011
0011	0010	0010
0100	0110	0111
0101	0111	0110
0110	0101	0100
0111	0100	0101
1000	1100	1111
1001	1101	1110
1010	1111	1100
1011	1110	1101
1100	1010	1000
1101	1011	1001
1110	1001	1011
1111	1000	1010

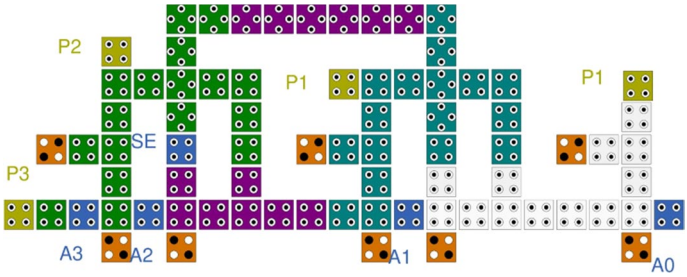


Fig. 11 The proposed irreversible 4-bit QCA B2G and vice versa

4.3 Proposed irreversible 8-bit B2G and vice versa

In this section, we design and simulate the irreversible structure of an 8-bit bit B2G code converter and vice versa in QCA technology. An 8-bit B2G code converter receives an 8-bit binary number on the input and delivers its equivalent gray code on the output. Alike, an 8-bit G2B conversion accepts an 8-bit gray number from input and delivers its equivalent binary code in output. Figure 12 shows the logic diagram for designing an 8-bit B2G and vice versa code converter. A_i*and* P_i are input and output, respectively. A_0. and A_7 are LSB and MSB, respectively. SEL is a converter selector. The design uses seven XOR gates and six multiplexer blocks. Equation (7) shows the relationship between inputs and outputs of the design. The design acts as a G2B converter if the value of SEL equals one. The circuit works as a B2G code converter if the value of SEL equals zero. Figure 13 indicates the QCA layout for the suggested irreversible 8-bit QCA B2G code converter and vice versa. A_i*and*. P_i are input and output, respectively. This circuit includes 204 cells, an area of 0.187μm^2, and three clock cycles.

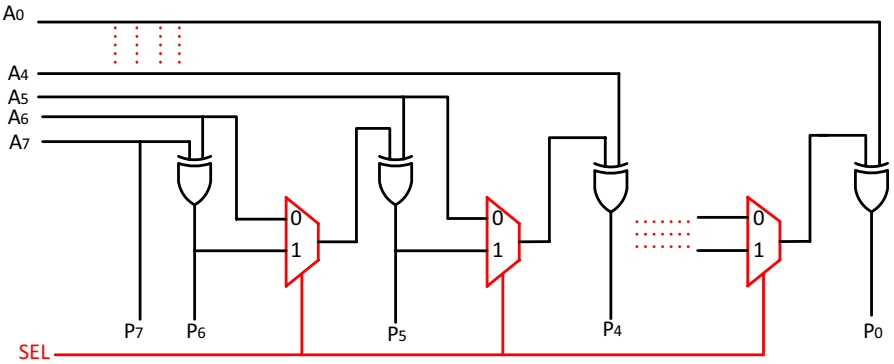


Fig. 12 The logic diagram of the irreversible 8-bit B2G code converter and vice versa

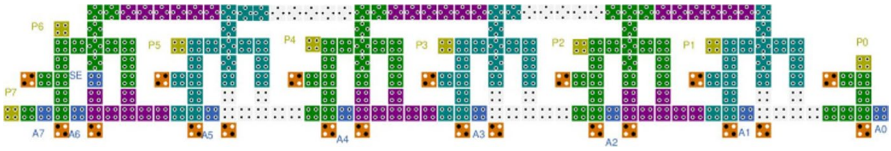


Fig. 13 The suggested irreversible 8-bit QCA B2G and vice versa

4.4 Proposed irreversible N-bit B2G and vice versa

In this section, we design and simulate an N-Bit B2G code converter and vice versa in QCA technology. Figure 14 shows the logic diagram for the N-bit code converter. The design uses N-1 XOR gates and N-2 multiplexer blocks. Equation (8) shows the relationship between inputs and outputs of the design.

$$\begin{cases} P_7 = A_7 \\ P_6 = A_6 \oplus A_7 \\ P_5 = A_5 \oplus \left(\overline{\text{SEL}}.A_6 \oplus \text{SEL}.\left(A_6 \oplus A_7\right)\right) \\ \cdots \\ \cdots \\ P_0 = A_0 \oplus \left(\overline{\text{SEL}}.A_1 \oplus \left(\text{SEL}.\left(A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus A_5 \oplus A_6 \oplus A_7\right)\right)\right) \end{cases} \tag{7}$$

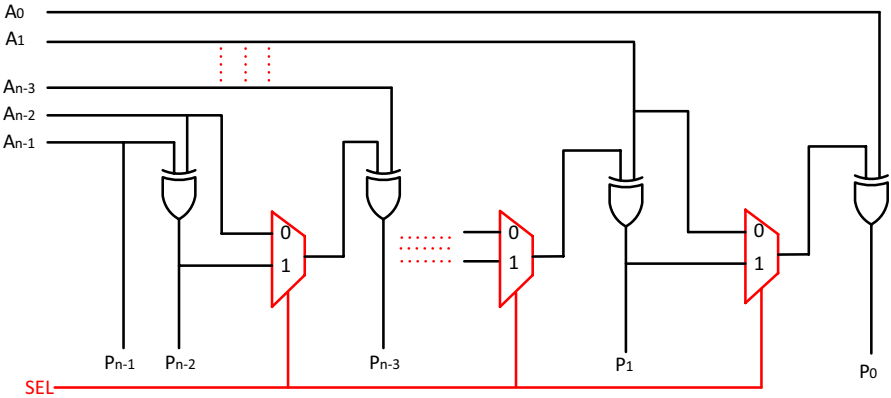


Fig. 14 The logic diagram for the irreversible N-bit B2G and vice versa

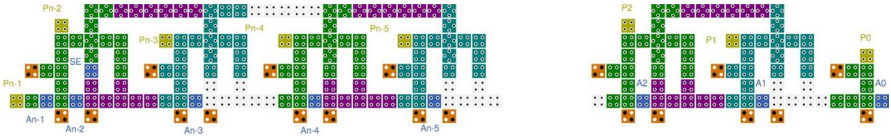


Fig. 15 The suggested irreversible N-bit QCA B2G and vice versa

Table 2 The equations for calculating figures of merit

Parameters	Equations
Total Number of Cells	$\text{Number}_{\text{Total}} = (\text{Number}_{\text{Total\_Mux}} * \text{Number\_Cell}_{\text{Mux}}) + (\text{Number}_{\text{Total\_Xor}} * \text{Number\_Cell}_{\text{Xor}})$
Total Area	$\text{Area}_{\text{Total}} = (\text{Number}_{\text{Total\_Mux}} * \text{Area}_{\text{Mux}}) + (\text{Number}_{\text{Total\_Xor}} * \text{Area}_{\text{Xor}})$
Total Clock Used	N -2

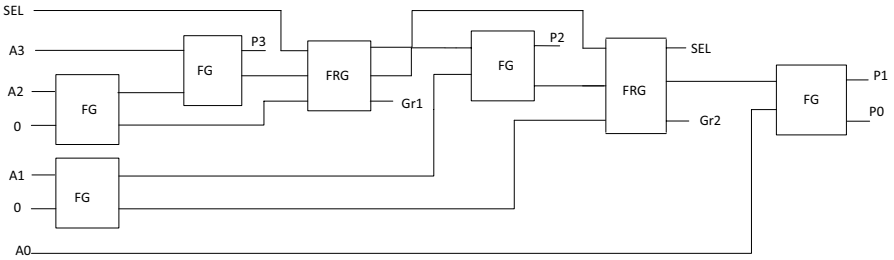
*Note that N is greater than or equal to 4

$$\begin{cases} P_{N-1} = A_{N-1} \\ P_{N-2} = A_{N-2} \oplus A_{N-1} \\ P_{N-3} = A_{N-3} \oplus \left(\overline{\text{SEL}}.A_{N-2} \oplus SEL.\left(A_{N-2} \oplus A_{N-1}\right)\right) \\ \ldots \\ \ldots \\ P_0 = A_0 \oplus \left(\overline{\text{SEL}}.A_1 \oplus \left(\text{SEL}.\left(A_1 \oplus A_2 \oplus A_3 \ldots\ldots\ldots\ldots\ldots \oplus A_{N-2} \oplus A_{N-1}\right)\right)\right) \end{cases} \tag{8}$$

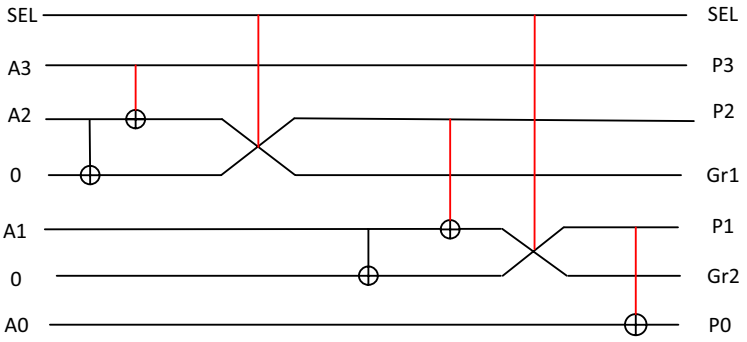
Figure 15 indicates the proposed irreversible N-bit B2G conversion and vice versa in QCA technology. A_i and P_i are inputs and outputs, respectively. We calculate the evaluation parameters, such as the number of cells, the occupied area, and the clocks for the N-bit state. The parameters used in the equations are defined as follows:

$\text{Number}_{\text{Total}}$: Total number of cells.
$\text{Number}_{\text{Total\_Mux}}$.: Total number of multiplexers.
$\text{Number\_Cell}_{\text{Mux}}$: Number of cells in each multiplexer.
$\text{Number}_{\text{Total\_Xor}}$: Total XOR.
$\text{Number\_Cell}_{\text{Xor}}$: Number of cells in each XOR.
$\text{Area}_{\text{Total}}$.: Total area of the structure.
Area_{mux}: Area of each multiplexer.
Area_{Xor}: Area of each XOR.

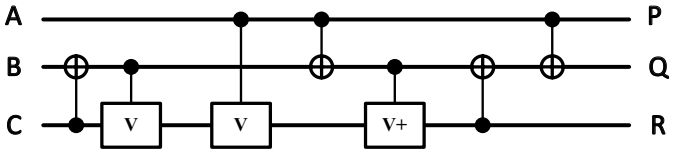
Table 2 indicates the general equations for calculating the cell counts, the area, and the clock numbers. In performed simulations, $\text{Number}_{\text{Total\_Mux}}$ and $\text{Number}_{\text{Total\_Xor}}$ are N-2 and N-1, respectively. For the mentioned equations in Table 2, the value of N is greater than or equal to 4.



(a) The block structureof the reversible 4-bit B2G code converter and vice versa



(b) The quantum structure of the reversible 4-bit B2G code converter and vice versa



(c) The quantum structure of the Fredkin gatein [32]

Fig. 16 The reversible 4-bit B2G converter and vice versa and quantum structure of Fredkin gate **a** The block structure of the reversible 4-bit B2G code converter and vice versa **b** The quantum structure of the reversible 4-bit B2G code converter and vice versa, **c** The quantum structure of the Fredkin gate in [30]

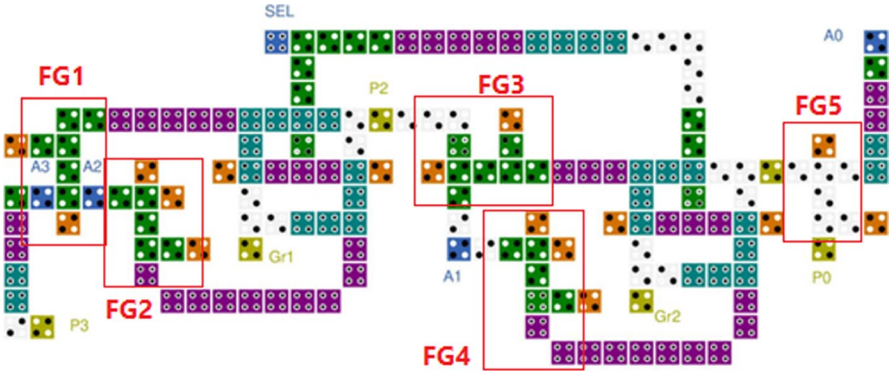


Fig. 17 Proposed reversible 4-bit QCA B2G and vice versa code converter

Table 3 The inputs and outputs of each Feynman gate

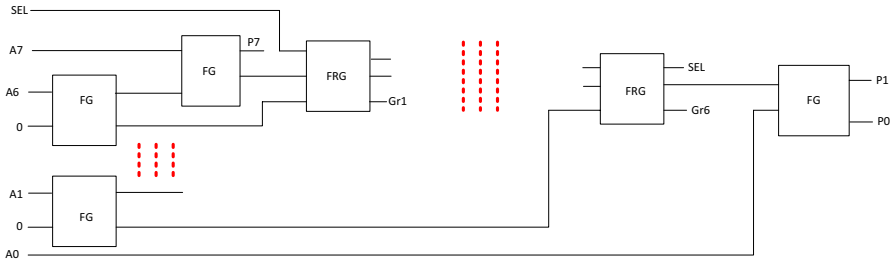
Label in Fig. 17	Inputs	Outputs
FG1	A_2, A_3	$P_3, A_2 \oplus A_3$
FG2	$0, A_2$	A_2, A_2
FG3	P_2, A_1	$P_2, P_2 \oplus A_1$
FG4	$0, A_1$	A_1, A_1
FG5	P_1, A_0	P_1, P_0

4.5 The suggested reversible 4-bit B2G and vice versa

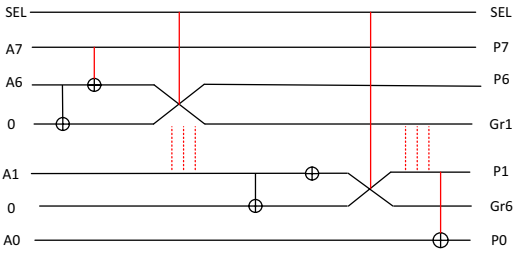
In this section, we design and simulate the structure of the reversible 4-bit B2G code converter and vice versa in QCA technology. Figure 16 shows the block and quantum structures of the reversible 4-bit B2G code converter and vice versa. Our structure uses five Feynman (FG) and two Fredkin blocks. The design acts as a 4-bit G2B converter if the value of SEL equals zero. Also, it works as a 4-bit B2G code converter if the value of SEL equals one. Figure 17 indicates the suggested reversible 4-bit QCA B2G converter and vice versa. This circuit requires 162 cells, an area of $0.19 \mu m^2$, and eight clock zones. For this design, the inputs and outputs of each Feynman are described in Table 3. The quantum structure of the Fredkin block is shown in Fig. 16. The quantum cost of the proposed Fredkin is five.

4.6 The suggested reversible 8-bit B2G and vice versa

In this section, we design and simulate the structure of the reversible 8-bit B2G code converter and vice versa in QCA technology. Figure 18 shows the block and quantum structures of the reversible 8-bit B2G and vice versa. Our structure uses 13 Feynman and six Fredkin blocks. The design acts as an 8-bit G2B code converter if the value of SEL equals zero. Also, it works as an 8-bit B2G code converter if the value of SEL equals one. Figure 19 indicates the suggested reversible 8-bit QCA B2G and vice versa.



(a) The block structure



(b) The quantum structure

Fig. 18 The structure of the reversible 8-bit B2G and vice versa **a** The block structure, **b** The quantum structure

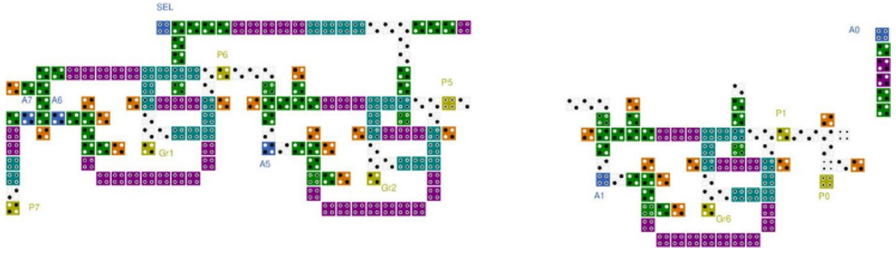
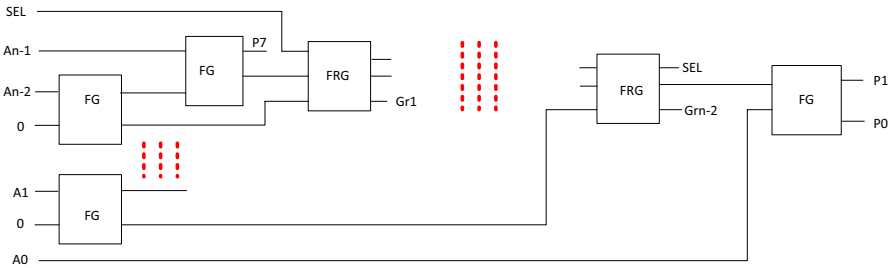


Fig. 19 Proposed reversible 8-bit QCA B2G and vice versa

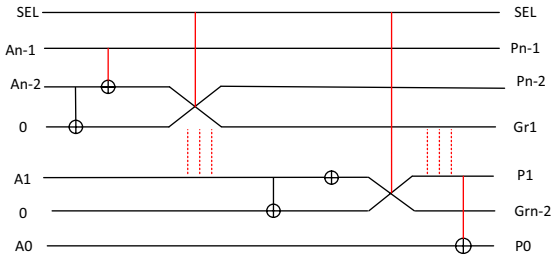
4.7 The suggested reversible N-bit B2G and vice versa

We design and simulate the proposed reversible N-bit B2G code converter and vice versa in QCA technology. Figure 20 shows the block and quantum structures of the reversible N-bit B2G and vice versa. Our structure uses 2 N-3 Feynman and N-2 Fredkin blocks. The design acts as an N-bit G2B code converter if the value of SEL equals zero. Also, it works as an N-bit B2G code converter if the value of SEL equals one.

Figure 21 indicates the proposed reversible N-bit QCA B2G code converter and vice versa. We calculate the figures of merit, including the cell counts, the area, and



(a) The block structure



(b) The Quantum structure

Fig. 20 The structure of the reversible N-bit B2G and vice versa. **a** The block structure, **b** The Quantum structure

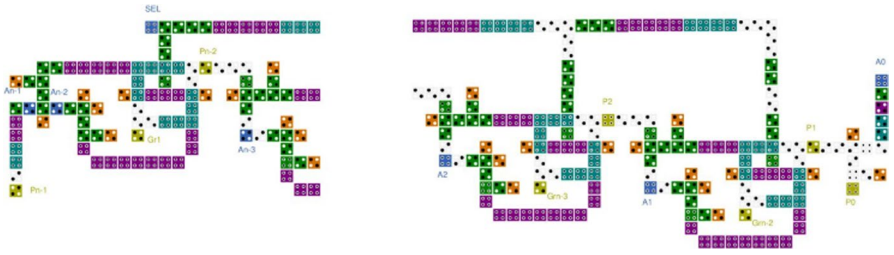


Fig. 21 Proposed reversible N-bit QCA B2G and vice versa

the clocks for the N-bit state. The parameters used in the equations are defined as follows:

$\text{Number}_{\text{Total\_cells}}$: Total number of cells.
$\text{Number}_{\text{Total\_Fredkins}}$: Total number of Fredkin.
$\text{Number\_Cell}_{\text{Fredkin}}$: Number of cells in each Fredkin.
$\text{Number}_{\text{Total\_Feynman}}$: Total Feynman.
$\text{Number\_Cell}_{\text{Feynman}}$: Number of cells in each Feynman.

$Number\_Cell_{SEL}$: The number of cells needed for connecting the selector line.
$Area_{Total}$: Total area of the structure.
$Area_{Fredkin}$: Area of each Fredkin.
$Area_{Feyman}$: Area of each Feynman.

Table 4 indicates the general equations for calculating the cell counts, the area, and the clock Used. In performed simulations, $Number_{Total\_Fredkin}$ and $Number_{Total\_Feyman}$ are N-2 and 2 N-3, respectively. For the mentioned equations in Table 4, the value of N is greater than or equal to 4.

5 Simulation result for the suggested 4-bit QCA B2G and vice versa

The simulation results for the proposed irreversible and reversible 4-bit B2G code converters are shown in Fig. 22 (a. and c.). In such a structure, the value of SEL is zero. As seen in simulation results, if the input value is 1010, i.e.,$A_3A_2A_1A_0 = 1010$, the output becomes 1111, i.e., $P_3P_2P_1P_0 = 1010$. Also, if the input value is 1111, i.e.,$A_3A_2A_1A_0 = 1111$, the output becomes 1000, i.e., $P_3P_2P_1P_0 = 1000$. The simulation result is verified based on Table 1. Figure 21 (b. and d.) shows the simulation results for the proposed irreversible and reversible 4-bit G2B code converters. In such a structure, the value of SEL equals one. As seen in simulation results, if the input value is 1010, i.e., $A_3A_2A_1A_0 = 1010$, the output becomes 1100, i.e., $P_3P_2P_1P_0 = 1100$. Also, if the input value is 1111, i.e., A3A2A1A0=1111, the output becomes 1010, i.e., $P_3P_2P_1P_0 = 1010$.

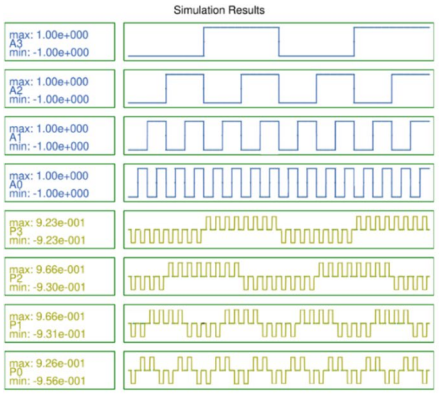
6 Discussion and Power dissipation analysis

In this section, we compare the proposed QCA structure of Fredkin gate and code converters with existing counterparts based on different figures of merit. Also, we show power dissipation of the proposed QCA irreversible and reversible 4-bit B2G and vice versa using QCADesigner-E [31].

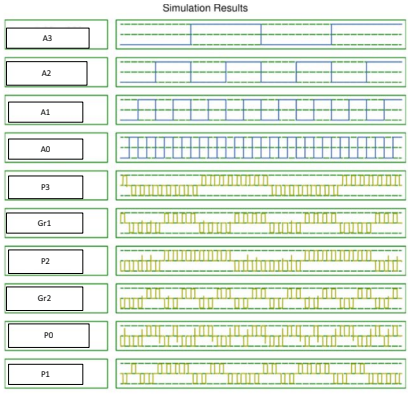
Table 4 The equations for calculating figures of merit

Parameters	Equations
Total Number of Cells	$Number_{Total} = (Number_{Total\_Fredkin} * Number\_Cell_{Fredkin}) + (Number_{Total\_Feyman} * Number\_Cell_{Feyman}) + Number\_Cell_{SEL}$
Total Area	$Area_{Total} = (Number_{Total\_Fredkin} * Area_{Fredkin}) + (Number_{Total\_Feyman} * Area_{Feyman})$
Total Clock Used	(N-2)/2

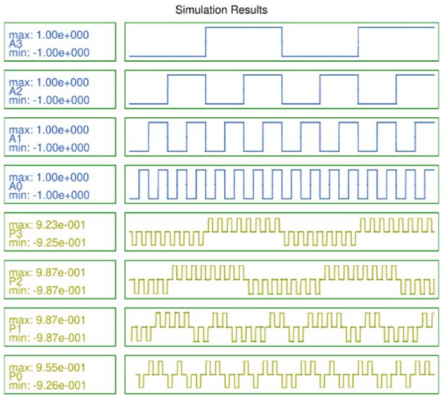
* Note that N is greater than or equal to 4



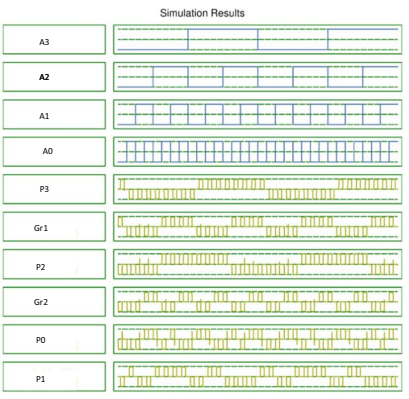
(a) The proposed irreversible 4-bit QCA B2G code converter



(c) The proposed reversible 4-bit QCA B2G code converter



(b) The proposed irreversible 4-bit G2B code converter



(d) The proposed reversible 4-bit QCA G2B code converter

Fig. 22 The simulation results for the proposed irreversible and reversible 4-bit B2G and vice versa in QCA. **a** The proposed irreversible 4-bit QCA B2G code converter, **b** The proposed irreversible 4-bit G2B code converter, **c** The proposed reversible 4-bit QCA B2G code converter, **d** The proposed reversible 4-bit QCA G2B code converter,

6.1 Discussion on Proposed Structures

Table 5 compares the proposed QCA structure for Fredkin gate with the existing works based on cell counts, area, and the number of clock zones. Results show that the proposed QCA layout of the Fredkin gate is more efficient than the existing works in terms of all figures of merit. The minimum improvement percentage with respect to the best existing design is computed and reported for all the evaluation parameters.

The QCA irreversible and reversible code converters are summarized in Tables 6 and 7. Also, these designs have been compared with each other based on metrics like the cell counts, the area, and clocks. As said before, the existing QCA circuits in the

Table 5 Comparing the proposed QCA Fredkin gate with the existing designs

Design	Number of cells	Number of clock zones	Area (μm^2)
[32]	100	4	0.12
[33]	73	3	0.060
[34]	42	3	0.042
[35]	80	3	0.14
[33]	73	3	0.065
[36]	105	6	0.09
Proposed	32	2	0.025
Minimum improvement Percentage (with respect to the best existing design)	23%	33%	40%

Table 6 Design summary of different non-reversible QCA code converters

Design	Number of cells	Clock used	Area (μm^2)
4-Bit B2G [22]	39	0.25	0.05
4-Bit B2G [23]	127	Not reported	0.41
4-Bit B2G [24]	99	0.75	Not reported
4-Bit G2B [24]	76	2.25	Not reported
4-Bit G2B [25]	69	0.75	0.10
4-Bit B2G [26]	33	0.5	0.0252
4-Bit G2B [26]	63	1	0.0566
4-Bit B2G [22]	39	0.25	0.05
4-Bit B2G (by quantum gate) [37]	44	0.5	0.08
4-Bit B2G (by classical gate 1) [37]	34	0.5	0.05
4-Bit B2G (by classical gate 2) [37]	356	2	0.57
4-Bit B2G (by classical gate 3) [37]	90	0.75	0.08
4-Bit B2G [38]	30	0.5	0.031
4-Bit B2G [39]	39	0.029	0.25
8-Bit B2G [26]	71	0.5	0.0556
8-Bit G2B [26]	139	2	0.1278
N-Bit B2G [26]	$33 + 38(0.25N - 1)$	0.5	$0.025 + 0.03(0.25N - 1)$
N-Bit G2B [26]	$63 + 76(0.25N - 1)$	N/4	$0.056 + 0.07(0.25N - 1)$

Table 7 Design summary of different reversible QCA code converters

Design	Number of cells	Area (μm^2)	Clock used	Number of cells
4-Bit B2G [25]	108	0.11	0.75	108
4-Bit G2B [25]	77	0.1	0.75	77
4-Bit B2G [40]	49	0.06	0.75	49
4-Bit G2B [40]	52	0.01	0.75	52

Table 8 Specifications of our proposed QCA B2G and vice versa circuits

Type	Number of bits	Number of cells	Clock used	Area	Constant input **	Garbage output **	Quantum cost **
Irreversible	4	75	1	0.08	–	–	–
	8	204	3	0.187	–	–	–
	N	$83 + (N-4) * 36$	N-2	$0.07 + (N-4) * 0.03$	–	–	–
Reversible	4	162	2	0.19	2	2	15
	8	484	6	0.67	6	6	43
	N	$160 + (N-4) * 80$	$N-2$	$(2) * 0.11$	N-2	N-2	(7*N)-13

*Note that N is greater than or equal to 4

** Applicable for the reversible designs

literature have just the ability to perform one of the B2G or G2B code conversions. Tables 6 and 7 show the existing QCA code converters based on the cell counts, the area, and the clocks used. Designs in Table 6 are non-reversible, whereas designs in Table 8 are reversible. Our proposed QCA circuits can perform both code conversions for N-bit *inputs*($N \geq 4$). For the mentioned equations in Table 8 (Proposed N-Bit), the value of N is greater than or equal to 4. Table 8 shows the specifications of our proposed QCA circuits, including quantum cost, constant input, garbage output, area, number of clocks, and the number of cells.

6.2 Power dissipation analysis

Researchers use the Hartree–Fock approximation to calculate the power dissipation of QCA cells. Equation (9) express the Hamiltonian matrix of an array of cells [17].

$$H = \begin{bmatrix} \frac{E_k}{2} \sum_i C_i f_{ij} & -\gamma \\ -\gamma & \frac{E_k}{2} \sum_i C_i f_{ij} \end{bmatrix} \tag{9}$$

where f_{ij} ,C_i, and E_k are geometrical parameter, polarization of the ith neighboring cell, and kink energy, respectively. According to Hamiltonian and Coherence vectors, the energy dissipated by a QCA cell is calculated as Eq. (10).

$$E_{\text{diss}} = \frac{h}{2} \int_{-T}^{T} \vec{\Gamma}.\frac{\overrightarrow{d\lambda}}{dt} dt \tag{10}$$

where Γ and λ are the energy environment vector and the coherence vector of the cell. The QCADesigner-E software is used to perform an energy dissipation analysis of the proposed structures, including total energy dissipation and average energy dissipation per cycle. In Table 9, the total energy dissipation and average energy dissipation per cycle of the proposed designs are shown.

Table 9 The energy dissipation of the proposed designs

Proposed design	Total energy dissipation (eV)	Average energy dissipation (eV)
Non-reversible 4 Bit	$6.07 * 10^{-2} J$	$5.52 * 10^{-3} J$
Reversible 4 Bit	$4.09 * 10^{-2} J$	$3.17 * 10^{-2} J$

7 Conclusion

In this paper, we proposed a novel high-performance QCA structure for the reversible Fredkin gate. We also proposed QCA converters capable of performing B2G and G2B code conversions. Designing such QCA structures with both capabilities in one single circuit is done for the first time. We proposed both reversible and non-reversible structures for those QCA code converters. Both 4-bit and 8-bit QCA B2G and vice versa code converters are presented. Then we extended it to N-bit QCA code conversion. The designs were simulated, and the simulation results were reported. These structures were compared to the existing designs regarding different figures of merits like the cell counts, the area, and the clocks. One of the advantages of our designs is their scalability. The proposed structure for the QCA Fredkin gate and other contributions of the paper can be exploited by other researchers in the field of quantum-dot cellular automata design.

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Authors' contributions All authors have contributed equally.

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Availability of data and materials Data sharing is not applicable to this article as no new data were created or analyzed in this study.

Declarations

Conflict of interest The authors declare that they have no competing interests.

Consent to participate Not applicable.

Consent for publication Not applicable.

Ethics approval Not applicable.

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